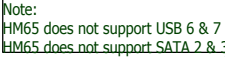


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05	SNB 2/4(DDR3 I/F)	1A	
06	SNB 3/4(POWER)	1A	
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08	PCH 1/6(DMI/FDI/VIDEO)	1A	
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10	PCH 3/6(PCIE/USB/CLK/NV)	1A	
11	PCH 4/6(GPIO/CPU/STRAP)	1A	
12	PCH 5/6(POWER)	1A	
13	PCH 6/6 (GND)	1A	
14	DDR3 DIMM-0-STD	1A	
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16	WPCE791L & FLASH	1A	
17	CRT/LVDS/CAMERA	1A	
18	CARD READER(RTS5209)	1A	
19	HDMI/THERMAL	1A	
20	USB	1A	
21	LAN (RTL8111F)	1A	
22	WLAN/KB-BL	1A	
23	HDD/ODD/G-SENSOR/TP/FAN	1A	
24	Audio ALC258-GR	1A	
25	LED/RF/PS	1A	
26	POWER +VCC_CORE (ISL95835)	1A	
27	POWER 3VPCU&RVCC5(PM6686)	1A	
28	POWER 1.5VSUS/VTT_MEM	1A	
29	POWER +1.05V(G5602R41U)-15A	1A	
30	POWER VCCSA/VCCIO	1A	
31	POWER VCC1.8/Thermal	1A	
32	POWER(BAT IN / ADA IN/ UL)	1A	
33	POWER CHARGER (ISL88731C)	1A	
34	POWER VGA_CORE(OZ8117)	1A	
35	POWER VGA_VCC1.8/VCC1.0	1A	
36	Thames_S3_PCIE	1A	
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41	HOLE/EMI/KB	1A	
42	IO PORT LIST	1A	
		1A	

* : No mount
E@ : For DIS GFX only
I@ : For INT GFX only

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Change List

P04--Add R441 51_4 for TDO.
P06--R183 & R188 change 100 +/- 5% to 100 +/- 1%.
P08-- R70 Don't Mount.
P09-- add R431 1M pull low.(For HDA_SYNC_R).
P09-- Add R442 [210/F_4] & R443[100/F_4] .(For PCH_JTAG_TDO_R).
P16-- Add KR57 10K_4 pull low. (For RSMRST#)
P24-- AR8 change from 22_4 to 0_4.(For ACZ_BITCLK)
P27-- PR345 change value from 22 to 220 ohm.(for +1.5V discharg)
P41-- Add C659,C660,C661,C662 [0.1U_4].(for DRAM module)

(2011/9/8)
P05--R172 [0 ohm] DNI; R171[0 ohm] Mount.(For DRAMRST_CNTRL_EC]
P08--R255 [0 ohm] DNI; R438 [0 ohm] Mount(For SUSACK#)
P08--R439 [0 ohm] DNI (For PCIE_WAKE#)
P08--R69 [0 ohm] DNI; R144[10K_4] (For DPWROK)
P12--R424 [0 ohm] DNI ; Q35 [2N7002] mount. (For +3_S5_DSW)
P12--Mount R428 [22 ohm]; R429 [1M_4]; C508[2200P_4]; Q36[DDTC144EUA]. (For +3_S5_DSW)
P16--KR56 [0 ohm] Mount(For PCIE_WAKE#)
P29--Add PQ291(For +5V_S5_DSW)
P29--PR356 pull high change from +5V_S5 to +5V_S5_DSW.
P29--PR362 pull high change from +5V_S5 to +5V_S5_DSW.
P29--PR365 pull high change from +5V_S5 to +5V_S5_DSW.
P29--PU104.15 pull high change from +5V_S5 to +5V_S5_DSW.

(2011/9/20)
P24--AR9 change value from 22 to 33 ohm.
P24--AC25 Don't mount
P27--PR314 change value from 470K to 0 ohm.
P27--PC453 delete
P28--PR367 change value from 820K to 470K.
P28--PR371 change value from 680K to 180K.
P28--PR372 change value from 20K to 100K.
P34--VPR49 change value from 20K to 0 ohm.
P35--VPR35 change value from 0 to 850K.
P35--VPC28 mount 0.01uF.

(2011/9/21)
P23--Add C670 0.1uF(For Freescale)

(2011/9/26)
P4--U7.5 change net from "+3V" to "+3V_S5".
P8--R253 change pull high from "+3V_S5_DSW" to "+3V_SUS".
P8--R103 change value from 1K/F to 1K/D.
P12-- Add C674[1uF]
P20--Add R445 [100K_4].
P23--U27.9 pin Net "HDD_INTERRUPT2" Cancel.
P26--KU1.26 change net from "HDD_INTERRUPT2" to "2540A_CTL3"

(2011/9/27)
P9--R49[33 ohm] & Q2[2N7002] mount.(for ACZ_SYNC)
P9--R432[0 ohm] no mount.(for ACZ_SYNC)
P19--Add U32,R447,R446,C675(Add Thermal sensor for HDD)

(2011/9/29)
P10--C359,C360 change value from 12PF to 15PF.
P16--Add KR58[100K]. (For DEEP_EC_EN pull high)
P37--VC82,VC83 change value to 27PF.(For VY1)
P40--mount VC460[330uF].(for +1.5V ripple)

(2011/9/30)
P8--Add R448[10K].(For PCIE_WAKE#_1 pull high)
P8--U16.E22 change Net to "DPWROK"
P16--KC17 don't Mount.(For 6237LDO5 glitch)
P16--KU1.77 change net to "DPWROK".
P16--Add KR59[100K] .(for DPWROK)
P16--Add KD9[RB501V-40].
P22--Add U33 (for 2nd source of KB Blight power) .
P27--Add PC676[0.01uF]. (Reduce SHDN noise)
P33--PC421 change from 10U/25V/X5R/1206 to 10U/25V/X5R_8.
P41--Add C677,C678,C679 [0.1uF].(For +3V_S5 Noise)

(2011/10/3)
P12--Q36 change to "2N7002".
P16--U2 change to "G9091-33".

P27--Add PQ295,PR514,PR516,PR515,PQ294,PC677,PR517,PR518,PR505(For DS3 power)
P42-- resaver EMI capa C680,C681,C682,C683,C684,C685,C686,C687 ,C688,C689,C690,C691,C692,C693,C694,C695,C696,C697,C698,C699,C700,C701,C702,C703,C704,C705,C706,C707,C708,C709,C710,C711,C712,C713

P08--U16.D10 cancel net"SLP_S5#".
P16--KU1.109 change net to"DEEP_EC_EN".
P16--KU1.83 cancel net "SLP_S5#"

(2011/10/4)
P10--Change "PCIE_REQ_CARD#" from U16.A8 to U16.V10.
P10--Delete R390,R391,R392
P10--Pin C46,C44,E40 add Net for thermal sensor test.
P19-- Add Q40,Q41,Q43,Q45 [PDTC144EU]
P19-- Add Q39,Q38,Q42,Q44 [2N7002DW]
P19-- Add R449,R450,R452,R453,R455,R456,R458,R459[100K]
P19-- Add R451,R454,R457,R460[22K].
P39--VR47 , VR49 change value to 240ohm.
P39--VR56 change value to 4.99K.
P39--VR55 change value to 51 ohm.

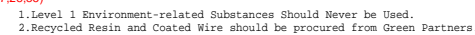
(2011/10/6)

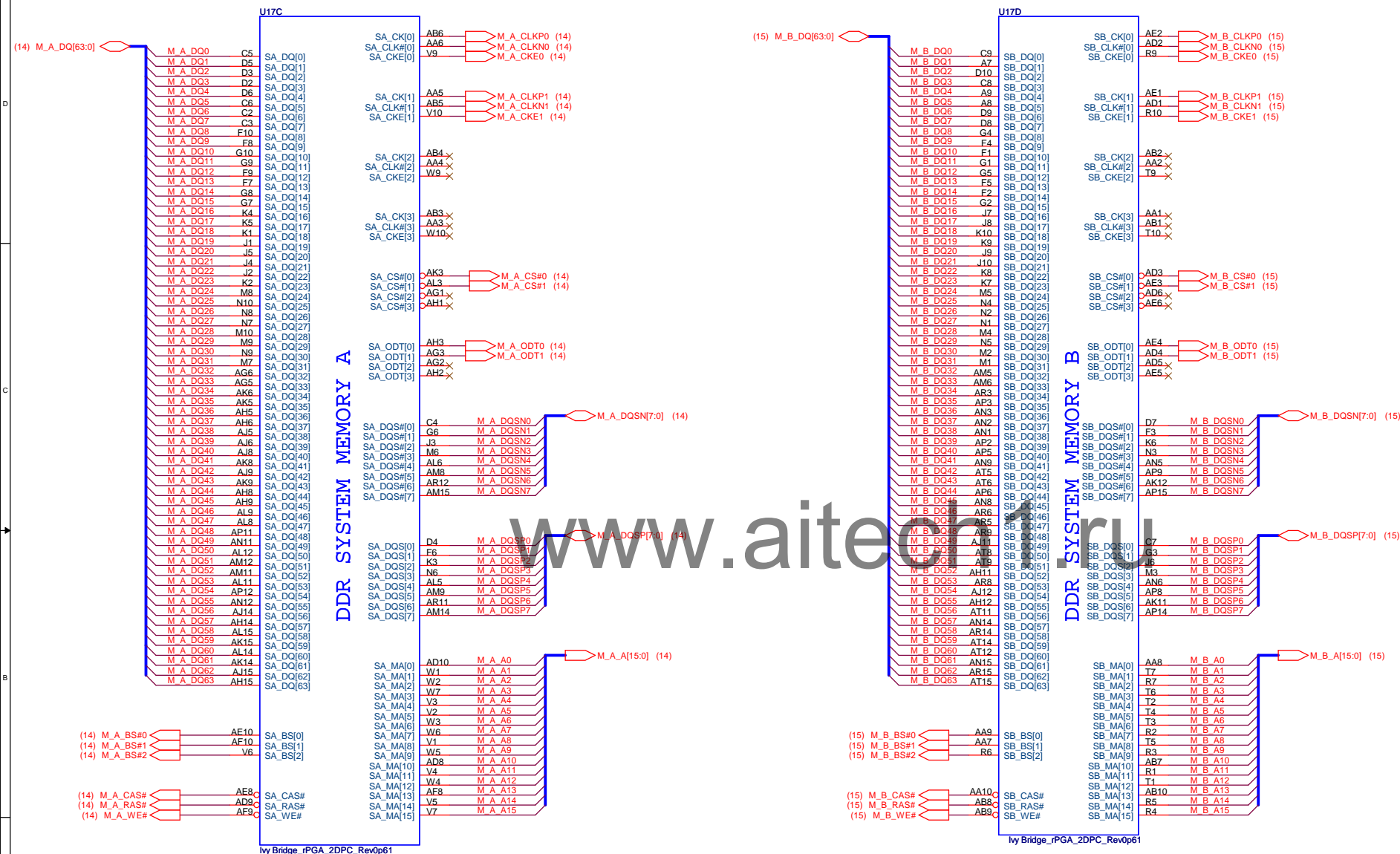
P23- reserver R461 ,R462 for TP SMBus

(2011/10/7)

P11- change R244 pull high source form +3V to +3V_S5

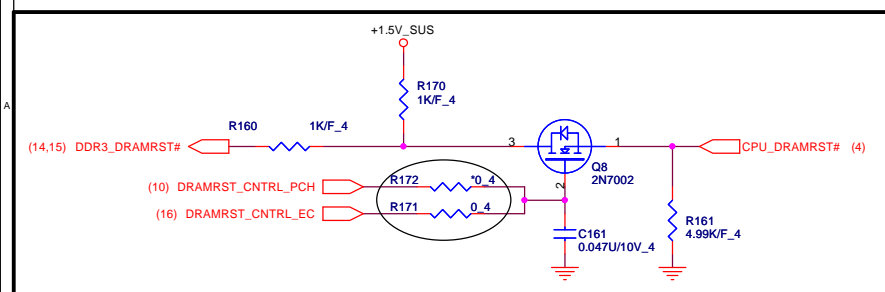
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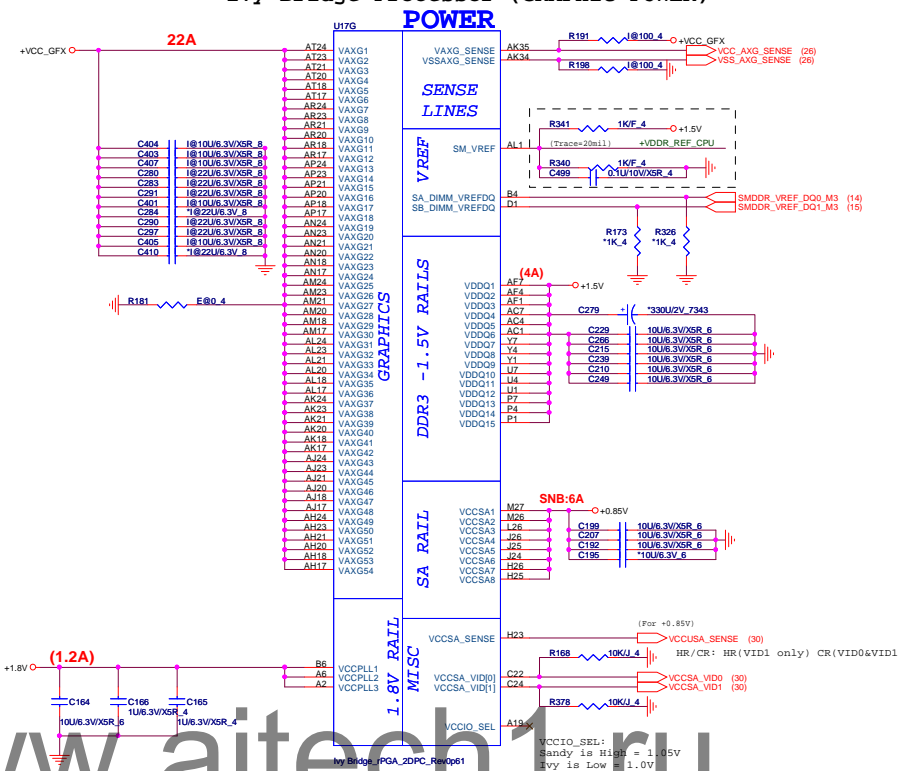
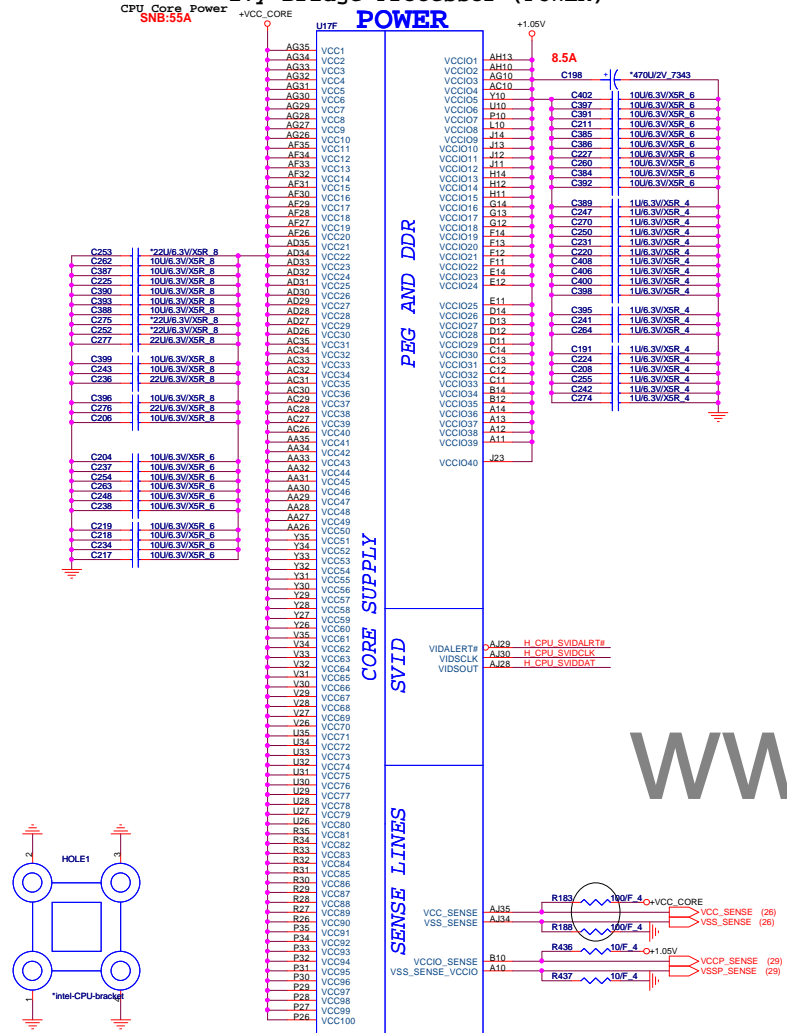




Ivy Bridge_rPGA_2DPC_Rev0p61

Ivy Bridge_rPGA_2DPC_Rev0p61





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Layout note: need routing together and ALERT need binding CLK and DATA

The diagram illustrates the routing for three SVID signals: SVID CLK, SVID DATA, and SVID ALERT. Each signal line is shown with its connection to a +1.05V supply and ground. A callout box for each signal indicates the placement of a pull-up resistor (R218, R347, R195) close to the VR pin. The signals are labeled as H_CPU_SVIDCLK, H_CPU_SVIDDATA, and H_CPU_SVIDALERT#.

SVID CLK

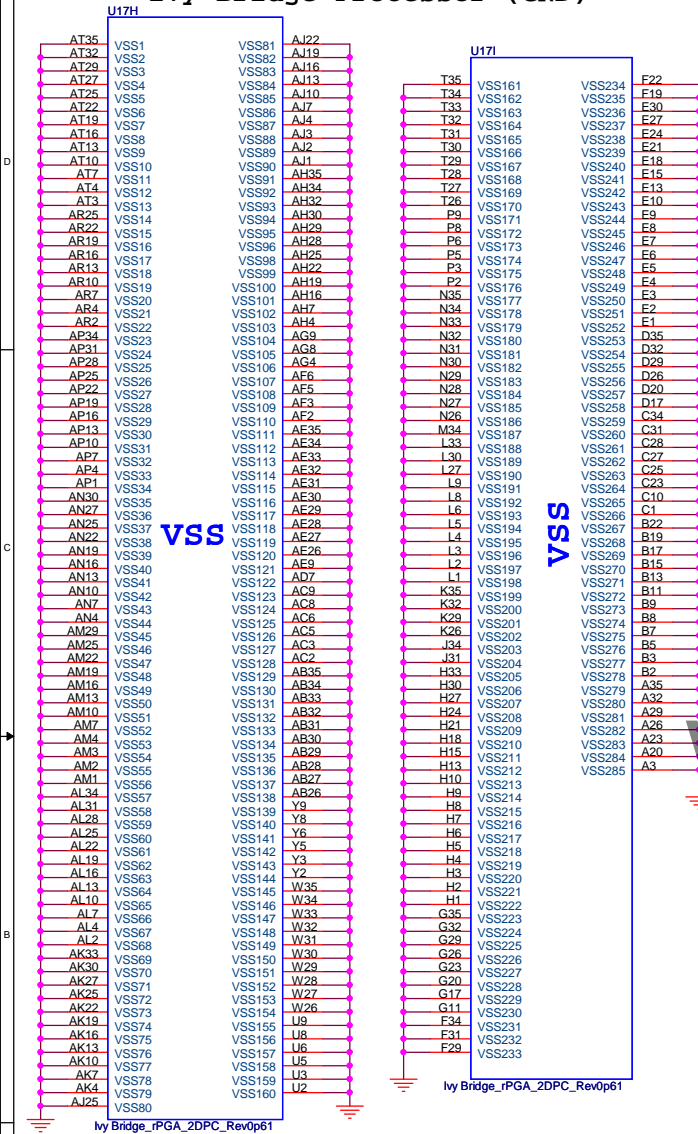
Close to VR

SVID DATA

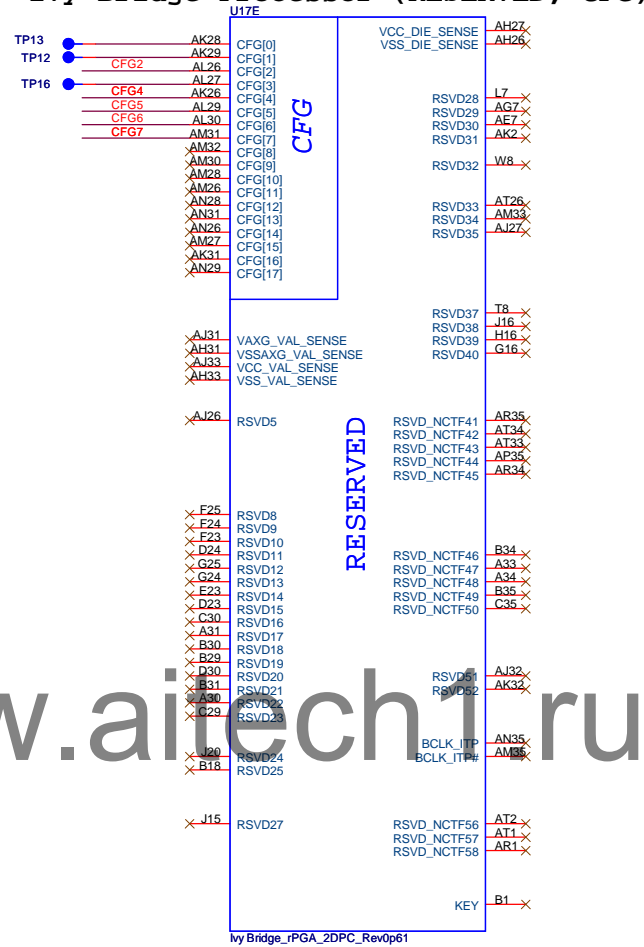
Close to VR

SVID ALERT

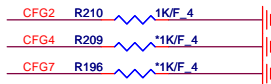
Ivy Bridge Processor (GND)



Ivy Bridge Processor (RESERVED, CFG)

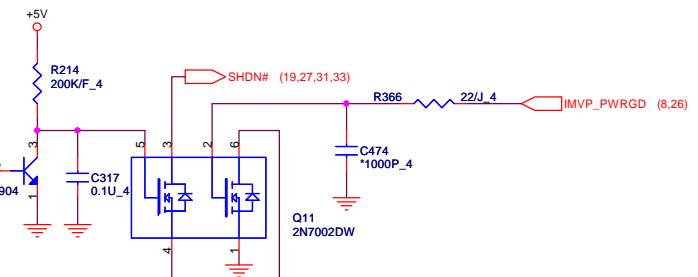


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CFG[6:5] (PCIe Port Bifurcation Straps)

11: (Default) x16 - X16 PEG interface
 10: PEG x8 x8 bifurcation enabled/disabled
 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

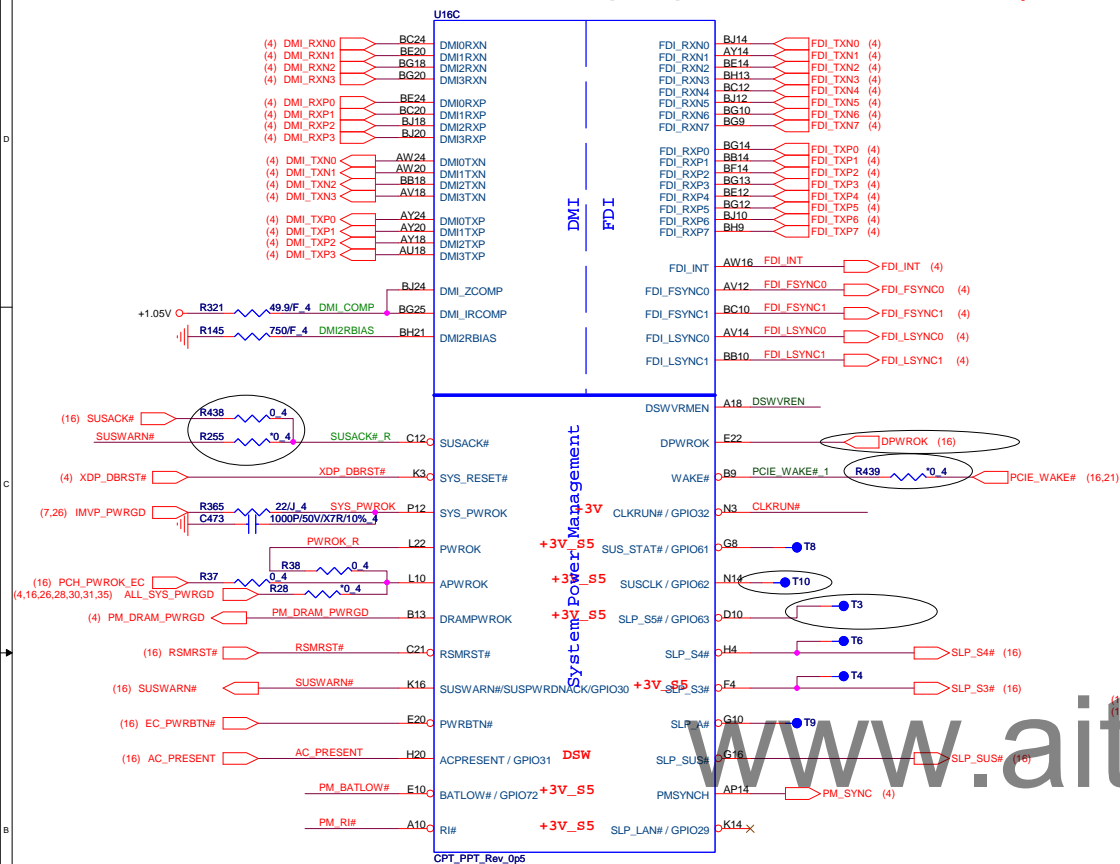
	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training



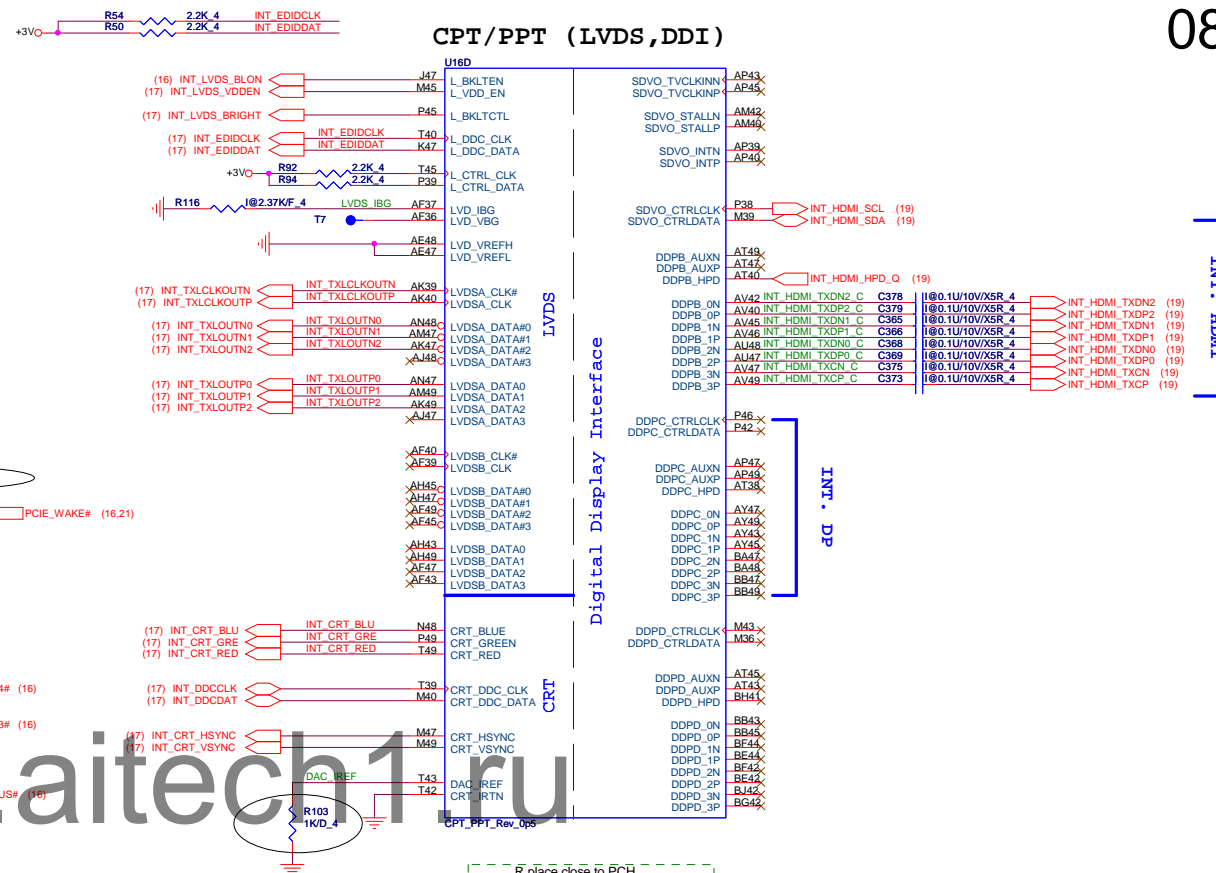
Quanta Computer Inc.
PROJECT : Chief River

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	SNB/IVB 4/4	1A
Date:	Wednesday, November 02, 2011	Sheet 7 of 42

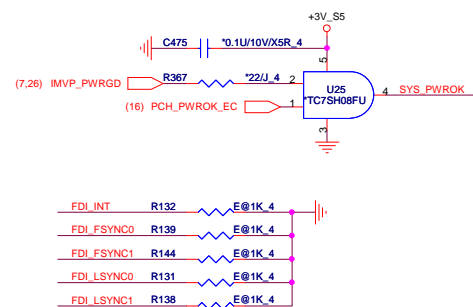
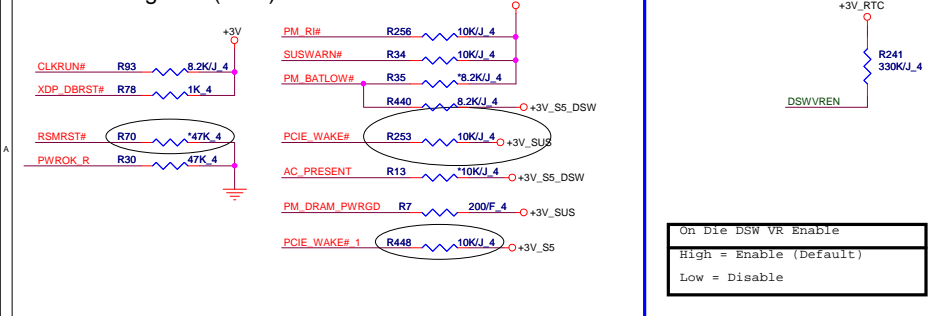
CPT/PPT (DMI, FDI, PM)



CPT/PPT (LVDS,DDI)

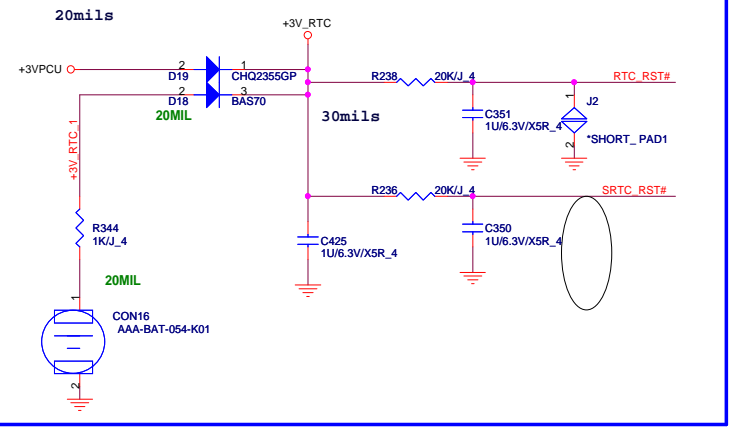


PCH Pull-high/low(CLG)



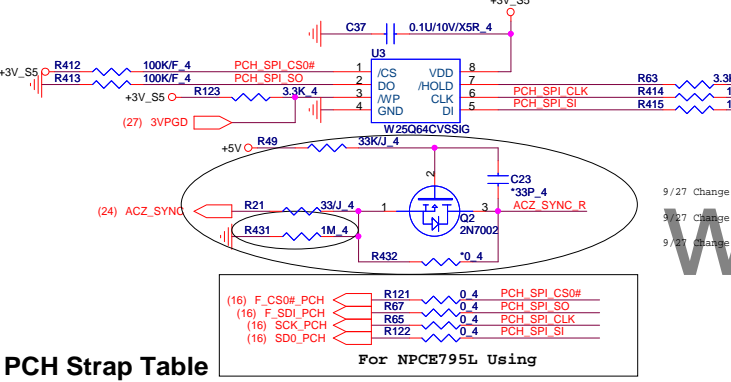
- 1.Level 1 Environment-related Substances Should Never be Used.
- 2.Recycled Resin and Coated Wire should be procured from Green Partners

RTC Circuitry(RTC)



MX25L3205DM2I-12G: AKE39FP0Z00
W25X32VSSIG: AKE39ZP0N00

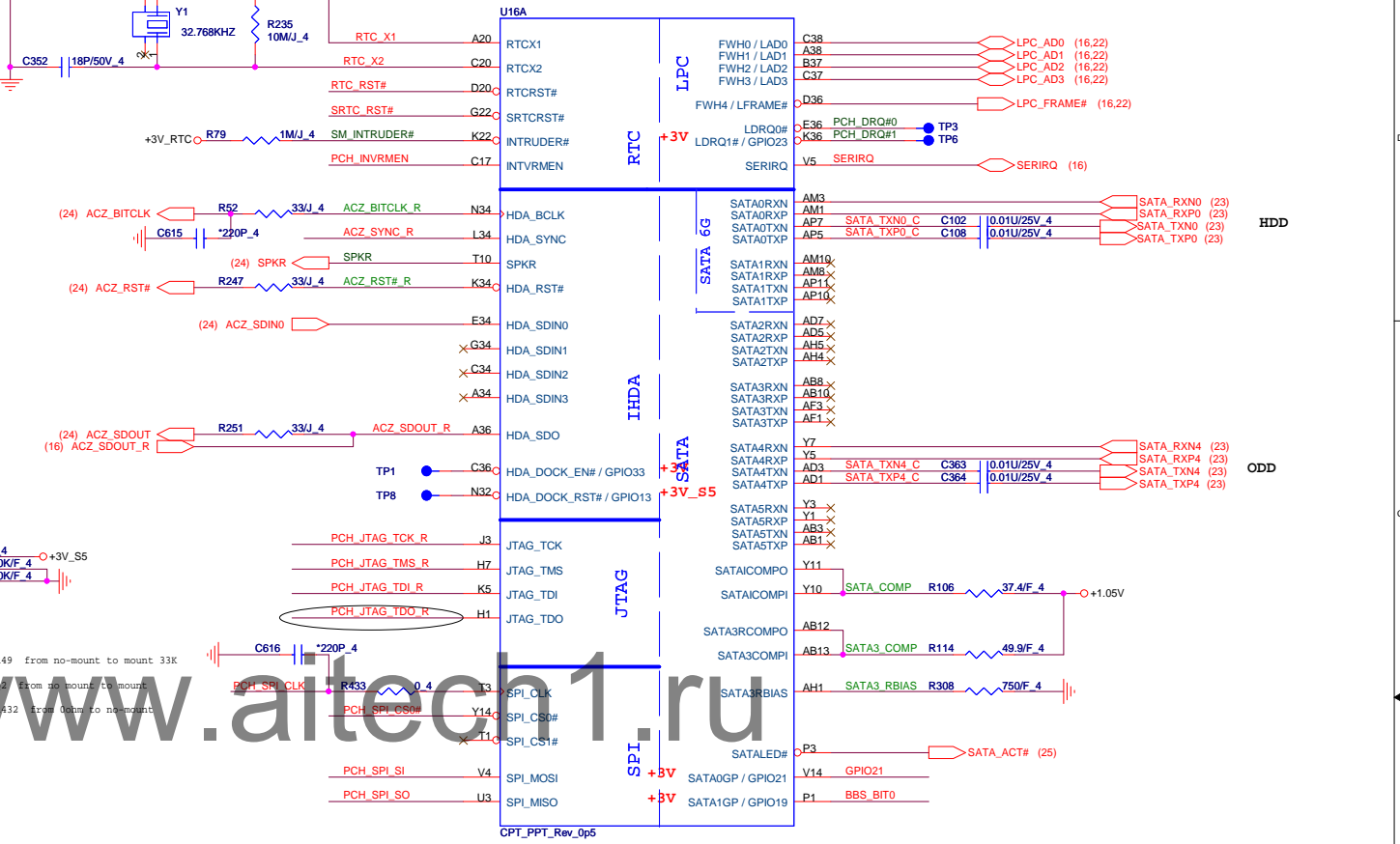
PCH SPI (CLG)



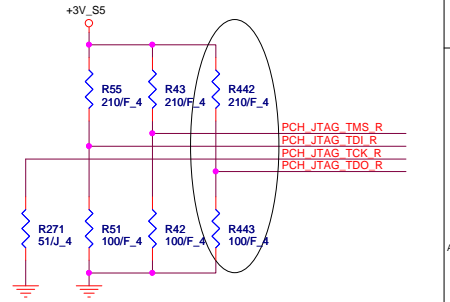
PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	HK1/HK2 note
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	SPKR
PCI_GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R270 1K_4 PCI_GNT3# (10)
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+3V_RTC R242 330K/J_4 PCH_INVRMEN
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	Default weak pull-up on GNT0/1# [Need external pull-down for LPC BIOS]	TP47 BBS_BIT1 (10) TP43 BBS_BIT0
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK		
HDA_SDO	Flash Descriptor Security	PWROK	0 = Default (weak pull-down 20K) 1 = Enabled	ACZ_SDOOUT_R R140 2.2K_4 +1.8V R320 1K_4 NV_CLE (11) H_SNB_IVB# (4)
DF_TVS	DMI/FDI Termination voltage	PWROK	0 = Set to Vss for Ivy Bridge 1 = Set to Vcc for Sandy Bridge (weak pull-down 20K)	TP44 PLL_ODVR_EN (11)
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	+3V_S5 R29 1K_4 ACZ_SYNC_R
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	

CPT/PPT (HDA,JTAG,SATA)



PCH JTAG Debug (CLG)



Quanta Computer Inc.
PROJECT : Chief River

Size	Document Number	Rev
	CPT/PPT 2/6	1A

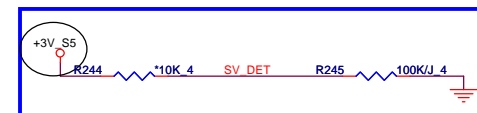
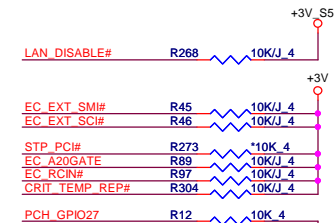
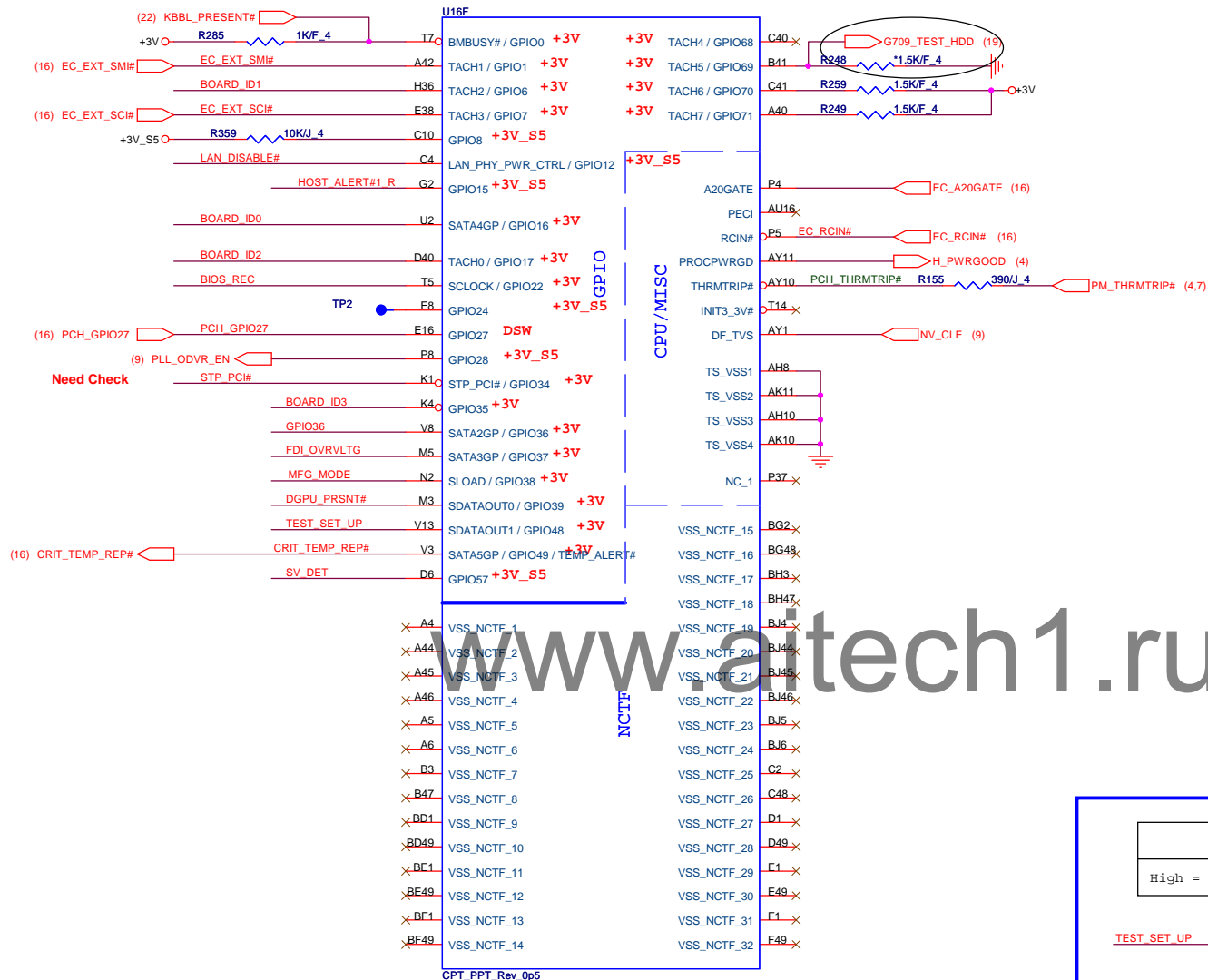
Date: Wednesday, November 02, 2011 Sheet 9 of 42

1.Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

CPT/PPT (GPIO,VSS_NCTF,RSVD)

GPIO Pull-up/Pull-down(CLG)

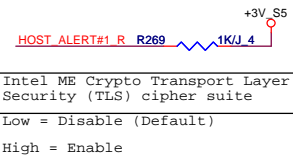
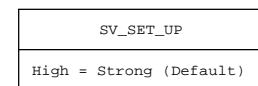
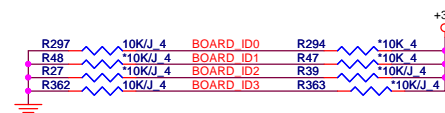
11



	R363(High) R362(Low)	R294(High) R297(Low)
Board ID3	Board ID0	
14"/HK6	0	0
15"/HK5	0	1
17"/HK7	1	0

Board ID1 (VRAM Vendor)	Samaung(1)	Hynix(0)
R47(High)	Stuff	No Stuff
R48(Low)	No Stuff	Stuff

Board ID2		
14" 4PCS	1G	512M
15" 8PCS	1G	2G
R39(High)	Stuff	No Stuff
R27(Low)	No Stuff	Stuff



MFG-TEST

MFG_MODE R287 10KJ 4



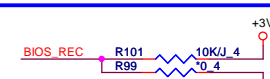
FDI TERMINATION
VOLTAGE
OVERRIDE

LOW - Tx, Rx terminated
to same voltage



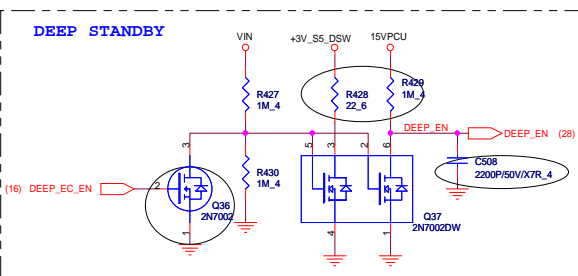
DMI TERMINATION
VOLTAGE
OVERRIDE

Low = Tx, Rx terminated to
same voltage (DC Coupling Mode)
(DEFAULT)



BIOS RECOVERY

High = Disable (Default)
Low = Enable



CPT/PPT (GND)

U16I

U16H		
H5	VSS[0]	
AA17	VSS[1]	VSS[80]
AA2	VSS[2]	VSS[81]
AA3	VSS[3]	VSS[82]
AA33	VSS[4]	VSS[83]
AA34	VSS[5]	VSS[84]
AB11	VSS[6]	VSS[85]
AB14	VSS[7]	VSS[86]
AB39	VSS[8]	VSS[87]
AB4	VSS[9]	VSS[88]
AB43	VSS[10]	VSS[89]
AB5	VSS[11]	VSS[90]
AB7	VSS[12]	VSS[91]
AC19	VSS[13]	VSS[92]
AC2	VSS[14]	VSS[93]
AC21	VSS[15]	VSS[94]
AC24	VSS[16]	VSS[95]
AC33	VSS[17]	VSS[96]
AC34	VSS[18]	VSS[97]
AC48	VSS[19]	VSS[98]
AD10	VSS[20]	VSS[99]
AD11	VSS[21]	VSS[100]
AD12	VSS[22]	VSS[101]
AD13	VSS[23]	VSS[102]
AD19	VSS[24]	VSS[103]
AD24	VSS[25]	VSS[104]
AD26	VSS[26]	VSS[105]
AD27	VSS[27]	VSS[106]
AD33	VSS[28]	VSS[107]
AD34	VSS[29]	VSS[108]
AD36	VSS[30]	VSS[109]
AD37	VSS[31]	VSS[110]
AD38	VSS[32]	VSS[111]
AD39	VSS[33]	VSS[112]
AD4	VSS[34]	VSS[113]
AD40	VSS[35]	VSS[114]
AD42	VSS[36]	VSS[115]
AD43	VSS[37]	VSS[116]
AD45	VSS[38]	VSS[117]
AD46	VSS[39]	VSS[118]
AD8	VSS[40]	VSS[119]
AE2	VSS[41]	VSS[120]
AE3	VSS[42]	VSS[121]
AE10	VSS[43]	VSS[122]
AE12	VSS[44]	VSS[123]
AD14	VSS[45]	VSS[124]
AD16	VSS[46]	VSS[125]
AF16	VSS[47]	VSS[126]
AF19	VSS[48]	VSS[127]
AF24	VSS[49]	VSS[128]
AF26	VSS[50]	VSS[129]
AF27	VSS[51]	VSS[130]
AF29	VSS[52]	VSS[131]
AF31	VSS[53]	VSS[132]
AF38	VSS[54]	VSS[133]
AF4	VSS[55]	VSS[134]
AF42	VSS[56]	VSS[135]
AF46	VSS[57]	VSS[136]
AF5	VSS[58]	VSS[137]
AF7	VSS[59]	VSS[138]
AF8	VSS[60]	VSS[139]
AG19	VSS[61]	VSS[140]
AG2	VSS[62]	VSS[141]
AG31	VSS[63]	VSS[142]
AG48	VSS[64]	VSS[143]
AH11	VSS[65]	VSS[144]
AH3	VSS[66]	VSS[145]
AH36	VSS[67]	VSS[146]
AH39	VSS[68]	VSS[147]
AH40	VSS[69]	VSS[148]
AH42	VSS[70]	VSS[149]
AH46	VSS[71]	VSS[150]
AH7	VSS[72]	VSS[151]
AJ19	VSS[73]	VSS[152]
AJ21	VSS[74]	VSS[153]
AJ24	VSS[75]	VSS[154]
AJ33	VSS[76]	VSS[155]
AJ34	VSS[77]	VSS[156]
AK12	VSS[78]	VSS[157]
AK3	VSS[79]	VSS[158]

CPT_PPT_Rev_0p5

U16I		
AY4	VSS[159]	VSS[259]
AY42	VSS[160]	VSS[260]
AY46	VSS[161]	VSS[261]
AY8	VSS[162]	VSS[262]
B11	VSS[163]	VSS[263]
B15	VSS[164]	VSS[264]
B19	VSS[165]	VSS[265]
B23	VSS[166]	VSS[266]
B27	VSS[167]	VSS[267]
B31	VSS[168]	VSS[268]
B35	VSS[169]	VSS[269]
B39	VSS[170]	VSS[270]
B7	VSS[171]	VSS[271]
F45	VSS[172]	VSS[272]
BB12	VSS[173]	VSS[273]
BB16	VSS[174]	VSS[274]
BB20	VSS[175]	VSS[275]
BB22	VSS[176]	VSS[276]
BB24	VSS[177]	VSS[277]
BB28	VSS[178]	VSS[278]
BB30	VSS[179]	VSS[279]
BB38	VSS[180]	VSS[280]
BB4	VSS[181]	VSS[281]
BB46	VSS[182]	VSS[282]
BC14	VSS[183]	VSS[283]
BC18	VSS[184]	VSS[284]
BC2	VSS[185]	VSS[285]
BC22	VSS[186]	VSS[286]
BC26	VSS[187]	VSS[287]
BC32	VSS[188]	VSS[288]
BC34	VSS[189]	VSS[289]
BC36	VSS[190]	VSS[290]
BC40	VSS[191]	VSS[291]
BC42	VSS[192]	VSS[292]
BC48	VSS[193]	VSS[293]
BD46	VSS[194]	VSS[294]
BD5	VSS[195]	VSS[295]
BE22	VSS[196]	VSS[296]
BE26	VSS[197]	VSS[297]
BE40	VSS[198]	VSS[298]
BF10	VSS[199]	VSS[299]
BF12	VSS[200]	VSS[300]
BF16	VSS[201]	VSS[301]
BF20	VSS[202]	VSS[302]
BF22	VSS[203]	VSS[303]
BF24	VSS[204]	VSS[304]
BF26	VSS[205]	VSS[305]
BF28	VSS[206]	VSS[306]
BD3	VSS[207]	VSS[307]
BF30	VSS[208]	VSS[308]
BF38	VSS[209]	VSS[309]
BF40	VSS[210]	VSS[310]
BF8	VSS[211]	VSS[311]
BG17	VSS[212]	VSS[312]
BG21	VSS[213]	VSS[313]
BG33	VSS[214]	VSS[314]
BG44	VSS[215]	VSS[315]
AT7	VSS[216]	VSS[316]
AU24	VSS[217]	VSS[317]
AU30	VSS[218]	VSS[318]
BH17	VSS[219]	VSS[319]
BH19	VSS[220]	VSS[320]
H10	VSS[221]	VSS[321]
BH27	VSS[222]	VSS[322]
BH31	VSS[223]	VSS[323]
BH33	VSS[224]	VSS[324]
BH35	VSS[225]	VSS[325]
BH39	VSS[226]	VSS[326]
BH43	VSS[227]	VSS[327]
BH7	VSS[228]	VSS[328]
D3	VSS[229]	VSS[329]
D12	VSS[230]	VSS[330]
D16	VSS[231]	VSS[331]
D18	VSS[232]	VSS[332]
D22	VSS[233]	VSS[333]
D24	VSS[234]	VSS[334]
D26	VSS[235]	VSS[335]
D30	VSS[236]	VSS[336]
D32	VSS[237]	VSS[337]
D34	VSS[238]	VSS[338]
D38	VSS[239]	VSS[339]
AY22	VSS[240]	VSS[340]
D8	VSS[241]	VSS[341]
E18	VSS[242]	VSS[342]
E26	VSS[243]	VSS[343]
G18	VSS[244]	VSS[344]
G20	VSS[245]	VSS[345]
G26	VSS[246]	VSS[346]
G28	VSS[247]	VSS[347]
G36	VSS[248]	VSS[348]
G48	VSS[249]	VSS[349]
H12	VSS[250]	VSS[350]
H18	VSS[251]	VSS[351]
H22	VSS[252]	VSS[352]
H24	VSS[253]	
H26	VSS[254]	
H30	VSS[255]	
H32	VSS[256]	
H34	VSS[257]	
F3	VSS[258]	

CPT_PPT_Rev_0p5

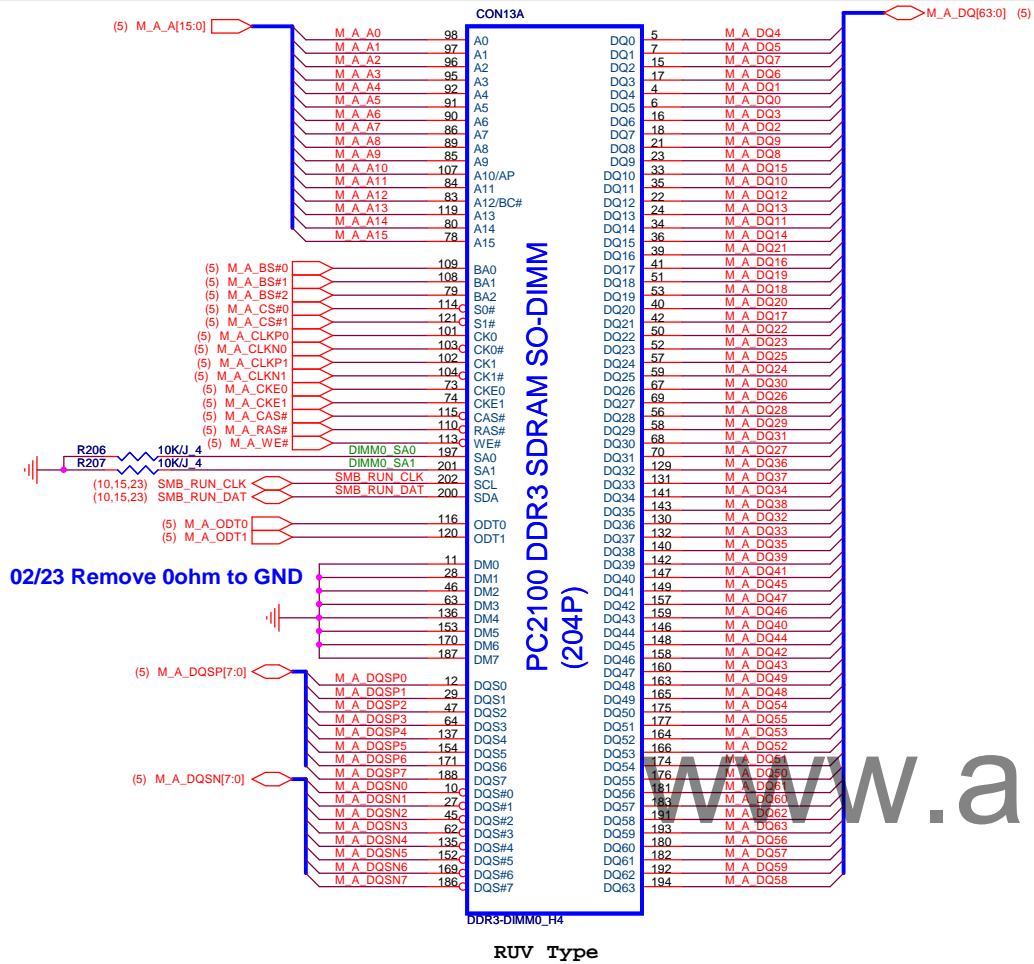
H46	VSS[259]
K18	VSS[260]
K26	VSS[261]
K39	VSS[262]
K46	VSS[263]
K7	VSS[264]
L18	VSS[265]
L2	VSS[266]
L20	VSS[267]
L26	VSS[268]
L28	VSS[269]
L36	VSS[270]
L48	VSS[271]
M12	VSS[272]
P16	VSS[273]
M18	VSS[274]
M22	VSS[275]
M24	VSS[276]
M30	VSS[277]
M32	VSS[278]
M34	VSS[279]
M38	VSS[280]
M4	VSS[281]
M42	VSS[282]
M46	VSS[283]
N8	VSS[284]
N18	VSS[285]
P30	VSS[286]
N47	VSS[287]
P11	VSS[288]
P18	VSS[289]
T33	VSS[290]
P40	VSS[291]
P43	VSS[292]
P47	VSS[293]
P7	VSS[294]
R2	VSS[295]
R48	VSS[296]
T12	VSS[297]
T31	VSS[298]
T37	VSS[299]
T4	VSS[300]
W34	VSS[301]
T46	VSS[302]
T47	VSS[303]
T8	VSS[304]
V11	VSS[305]
V17	VSS[306]
V26	VSS[307]
V27	VSS[308]
V29	VSS[309]
V31	VSS[310]
V36	VSS[311]
V38	VSS[312]
V43	VSS[313]
V7	VSS[314]
W12	VSS[315]
W19	VSS[316]
W2	VSS[317]
W27	VSS[318]
W48	VSS[319]
Y12	VSS[320]
Y38	VSS[321]
Y4	VSS[322]
Y42	VSS[323]
Y46	VSS[324]
Y8	VSS[325]
BG29	VSS[326]
N24	VSS[327]
AJ3	VSS[328]
AD47	VSS[329]
B43	VSS[330]
BE10	VSS[331]
BG41	VSS[332]
G14	VSS[333]
H16	VSS[334]
T36	VSS[335]
BG22	VSS[336]
BG24	VSS[337]
C22	VSS[338]
AP13	VSS[339]
M14	VSS[340]
AP3	VSS[341]
AP1	VSS[342]
BE16	VSS[343]
BC16	VSS[344]
BG28	VSS[345]
BJ28	VSS[346]



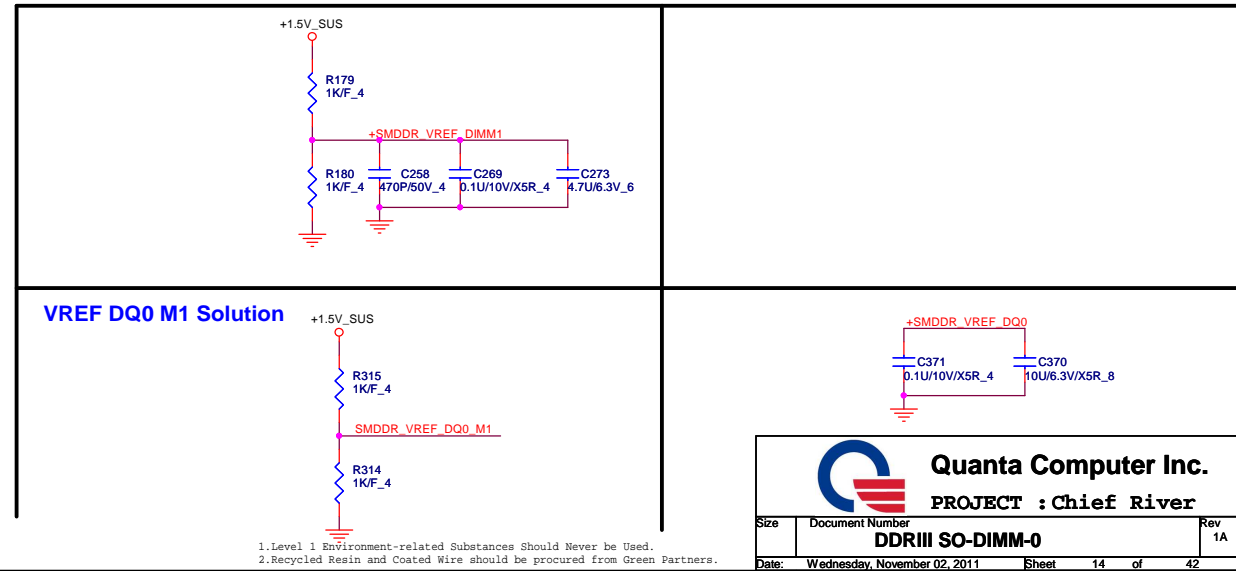
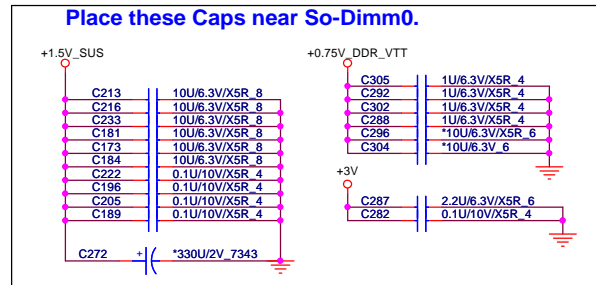
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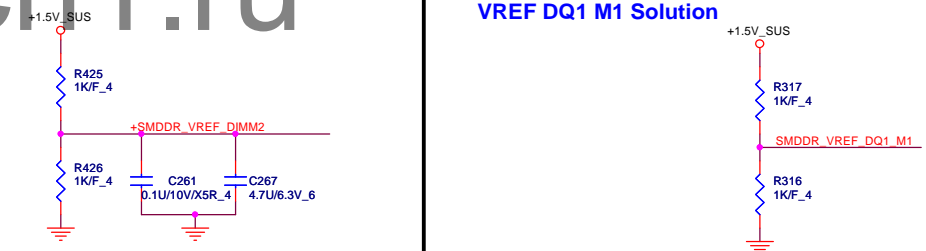
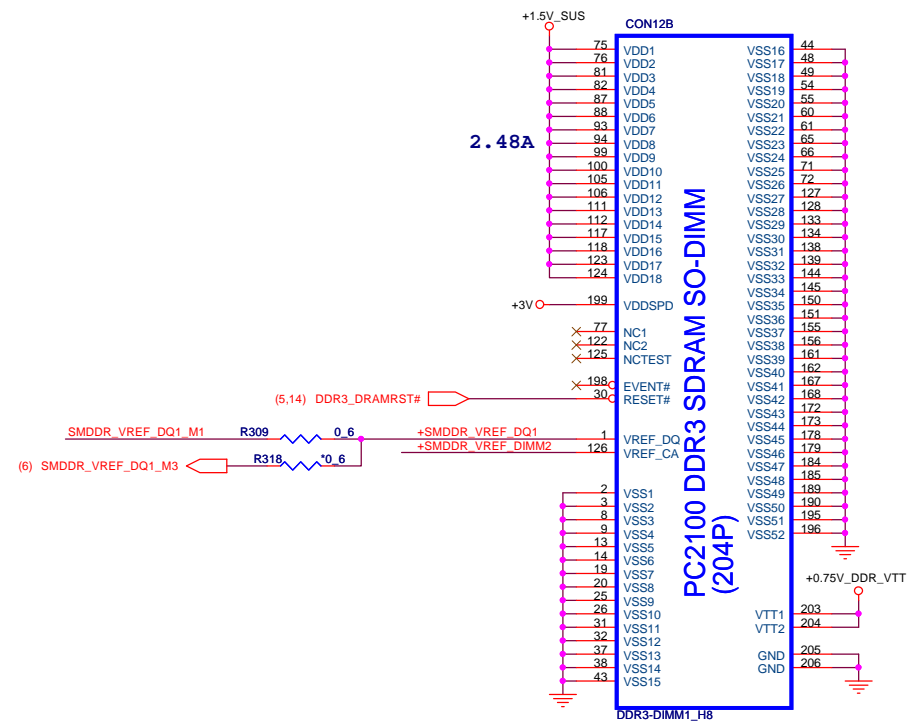
PROJECT : Chief River

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02/23 Remove 0ohm to GND



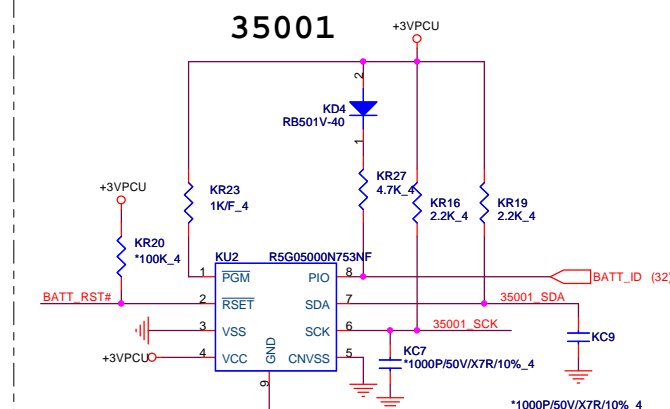
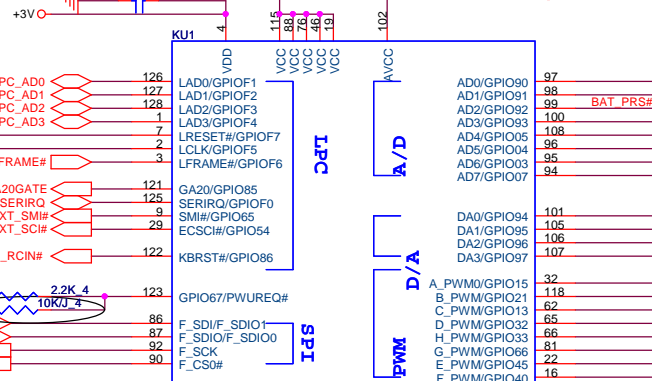


+1.5V_SUS
 C176 10U/6.3V/X5R_8
 C226 10U/6.3V/X5R_8
 C235 10U/6.3V/X5R_8
 C178 10U/6.3V/X5R_8
 C193 10U/6.3V/X5R_8
 C190 10U/6.3V/X5R_8
 C203 0.1U/10V/X5R_4
 C257 0.1U/10V/X5R_4
 C177 0.1U/10V/X5R_4
 C245 0.1U/10V/X5R_4
 +3V
 C285 2.2U/6.3V/X5R_6
 C286 0.1U/10V/X5R_4
 C295 1U/6.3V/X5R_4
 C293 1U/6.3V/X5R_4
 C294 1U/6.3V/X5R_4
 C298 1U/6.3V/X5R_4
 C299 10U/6.3V/X5R_6
 C301 *10U/6.3V_6
 C372 0.1U/10V/X5R_4
 C374 10U/6.3V/X5R_8

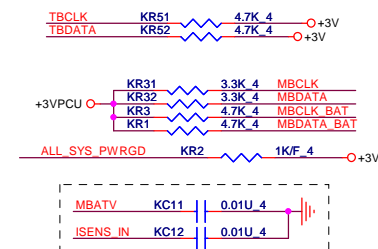
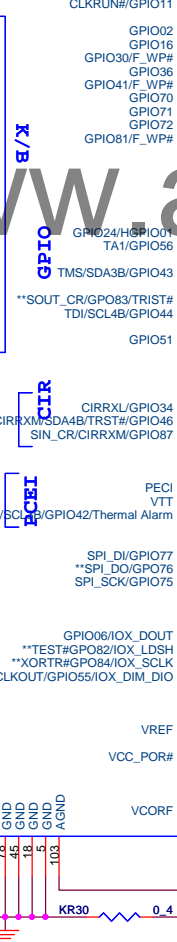
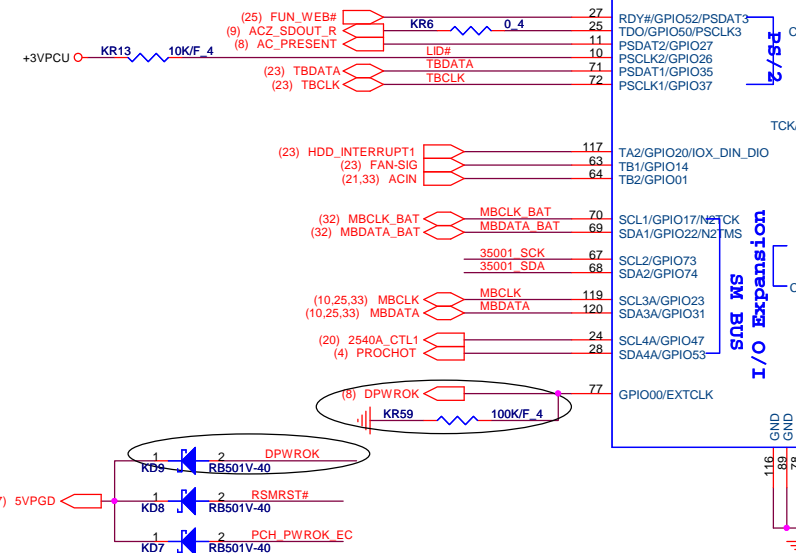
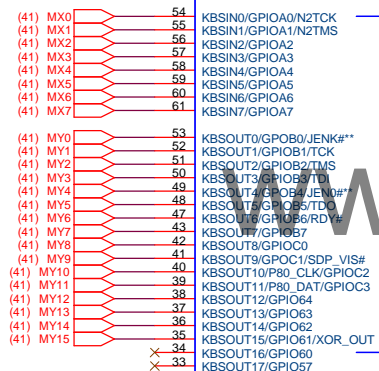
9/29 Del KC17 10U 0805

+3VPCU

KC17	*10U/6.3V/X5R 8
KC5	0.1U/10V/X5R 4
KC2	0.1U/10V/X5R 4
KC14	0.1U/10V/X5R 4
KC8	0.1U/10V/X5R 4
KC3	0.1U/10V/X5R 4
KC10	0.1U/10V/X5R 4



NPCE885L

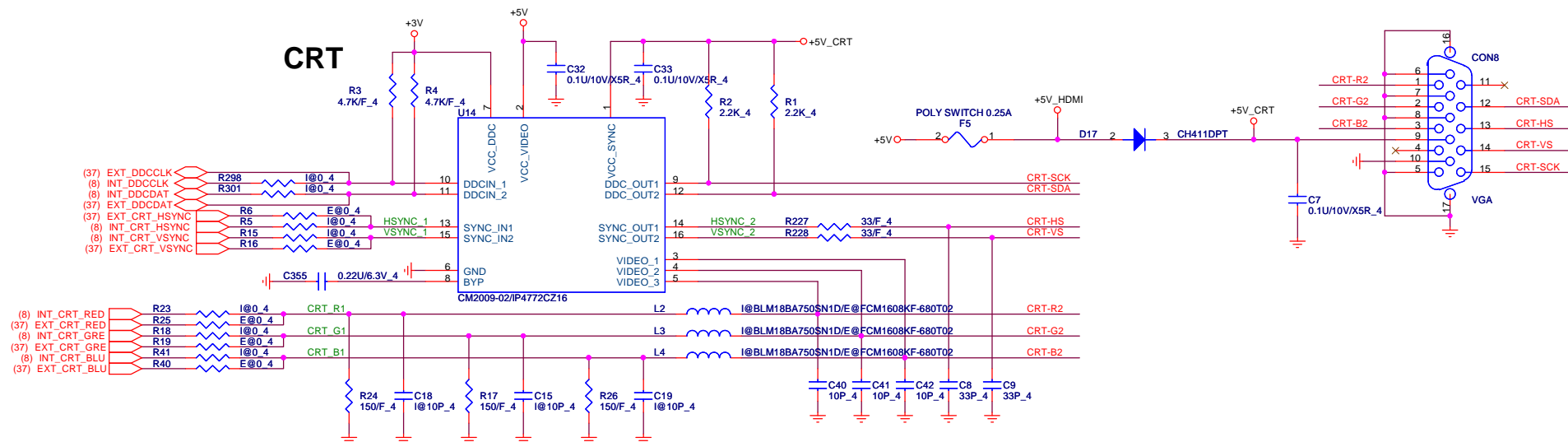


PROJECT : Chief River

NPCE885L

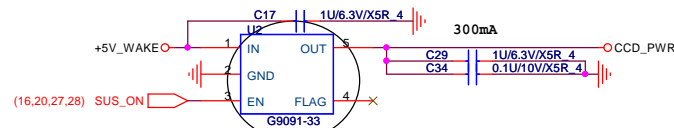
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CRT

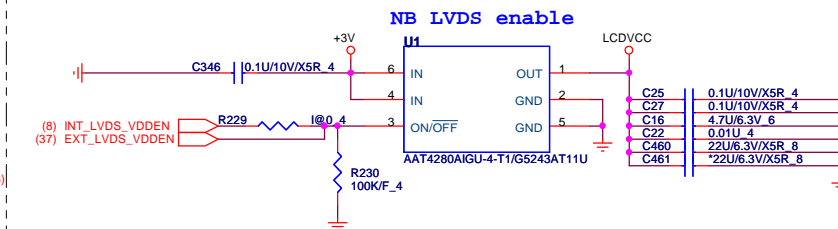
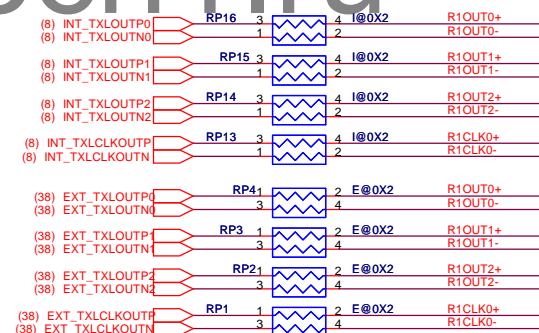
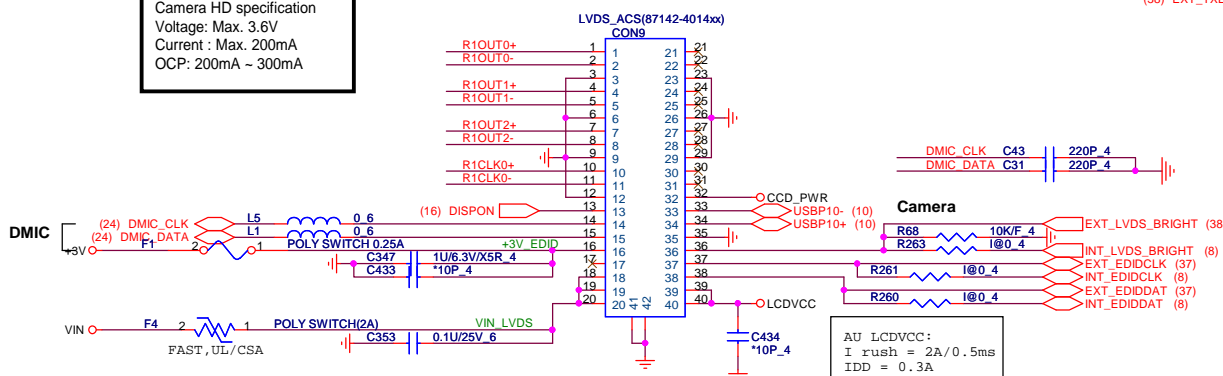


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USB Camera Power



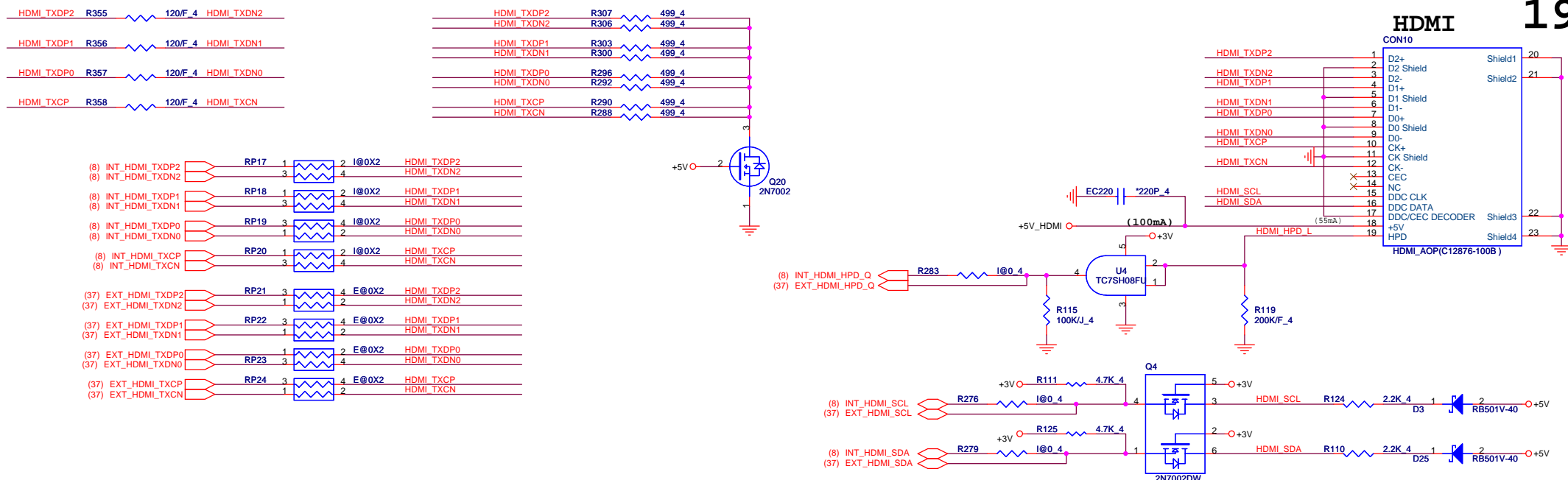
Camera HD specification
Voltage: Max. 3.6V
Current : Max. 200mA
OCP: 200mA ~ 300mA



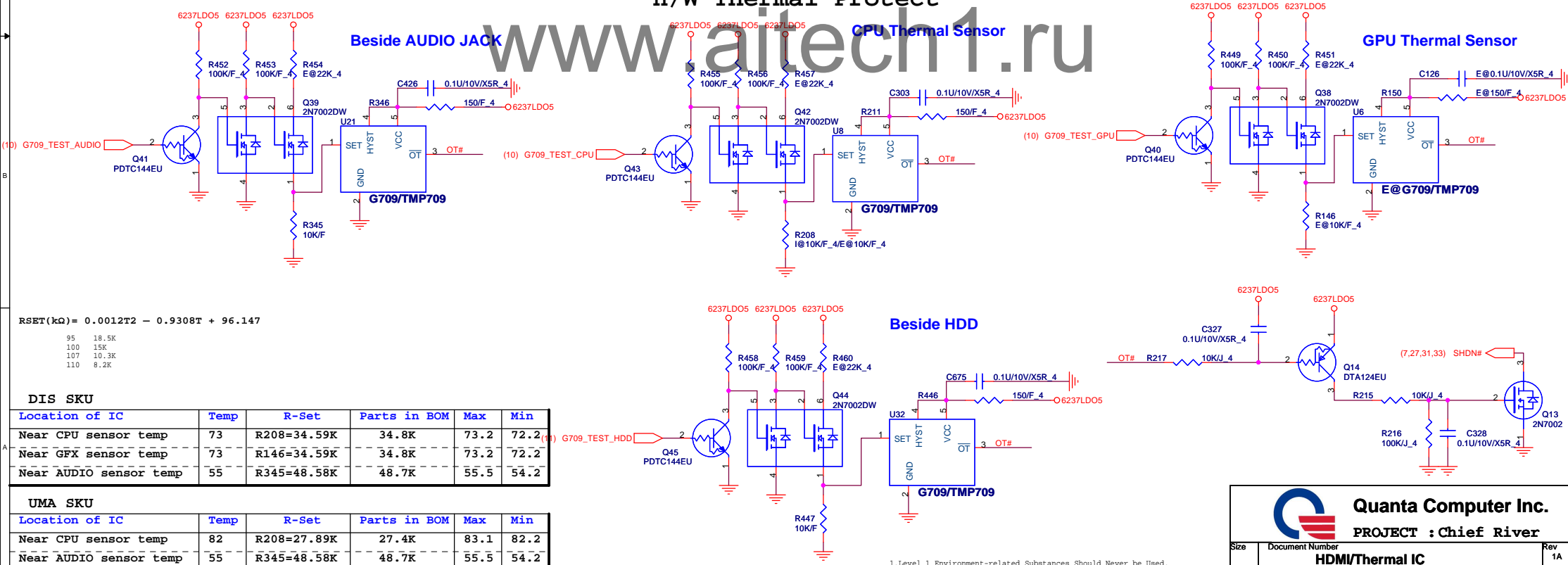
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PROJECT : Chief River

CRT/LVDS

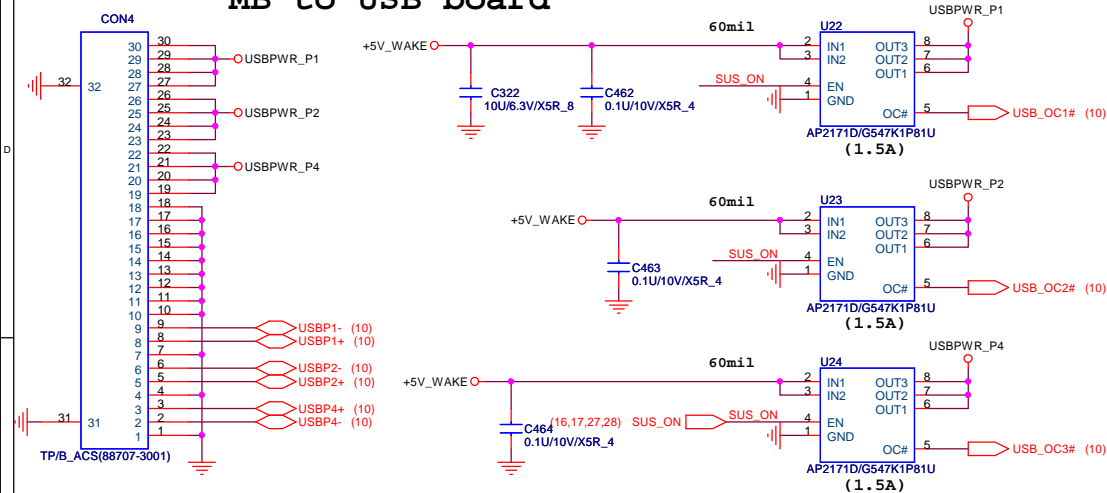




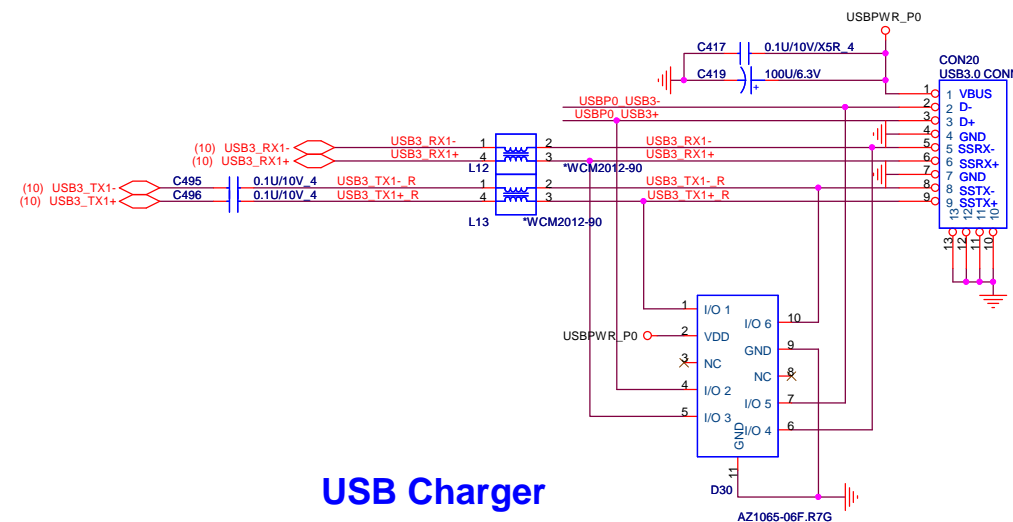
H/W Thermal Protect



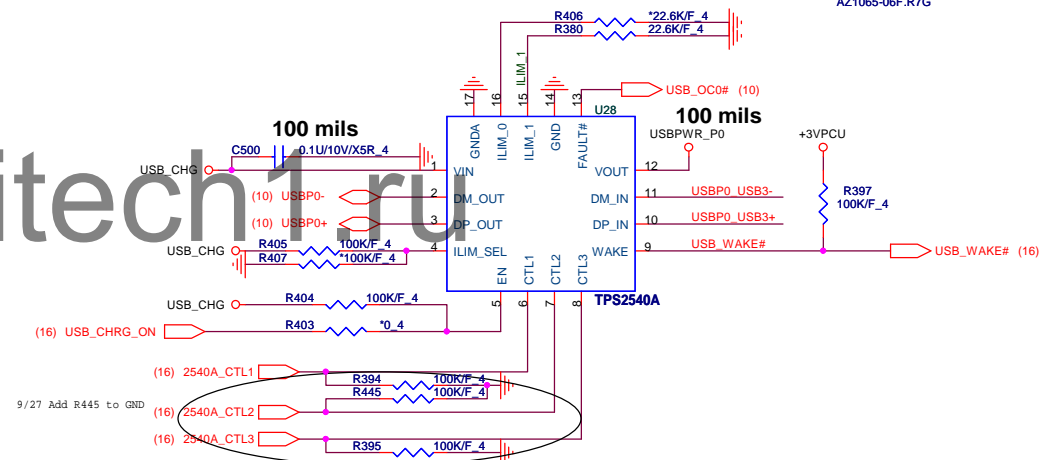
MB to USB board



USB 3.0 PORT0



USB Charger

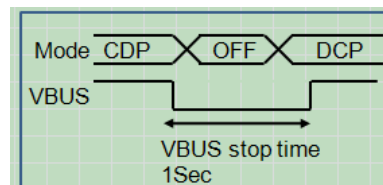


CTL_1	CTL_2	CTL_3	TPS 2540A/2543 Truth Table
0	0	0	OUT discharge, power switch OFF
0	X	1	DCP, Auto-detect(S3/S4/S5, 1.5A)
X	1	0	SDP, USB2.0 mode(S0, 0.5A)
1	0	0	DCP, BC SPEC1.2 only(S3/Deep standby/S4/S5, 1.5A)
1	0	1	DCP, Divider mode only(S3/S4/S5, 1.5A)
1	1	1	CDP (S0, 1.5A)

System State	USB Battery Charging Setting	
	Disable	Enable
S0	SDP	CDP
S3	SDP	DCP
Deep Standby	SDP (VBUS OFF)	DCP
S4	SDP (VBUS OFF)	DCP
S5	SDP (VBUS OFF)	DCP

SDP : Standard Downstream Port
 CDP : Charging downstream port
 DCP : Dedicated Charging Port
 Enable/Disable : setting by BIOS

port mode change, VBUS must be stopped for 1s



DCP: BC 1.2 only.

1. Level 1 Environment-related Substances Should Never be Used.
 2. Recycled Resin and Coated Wire should be procured from Green Partners.

USB WAKE

1	No device plug(LDO)
0	Device plug(Switch Power)

ILIM_SEL (I LIMIT(A)= 48000/R)

HI	I_LIM_1	
LO	I_LIM_0	48000/22.6K=2.123A

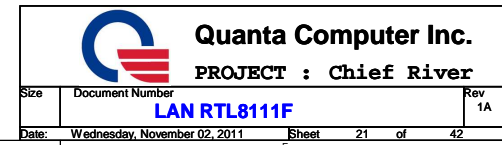


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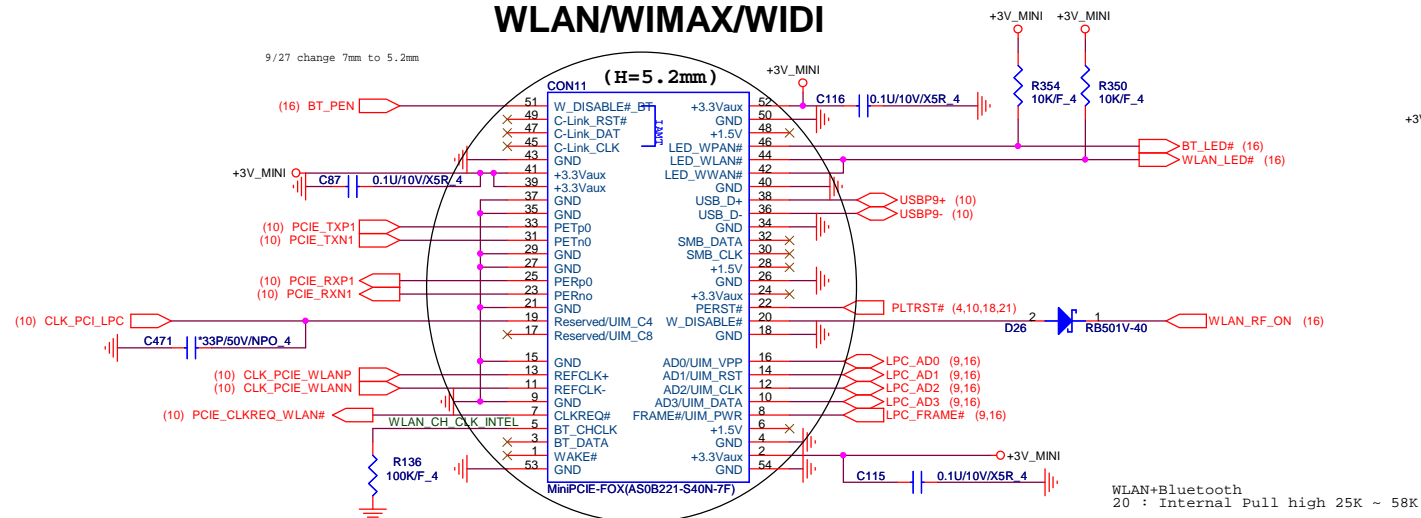
PROJECT : Chief River

USB/USB Charger

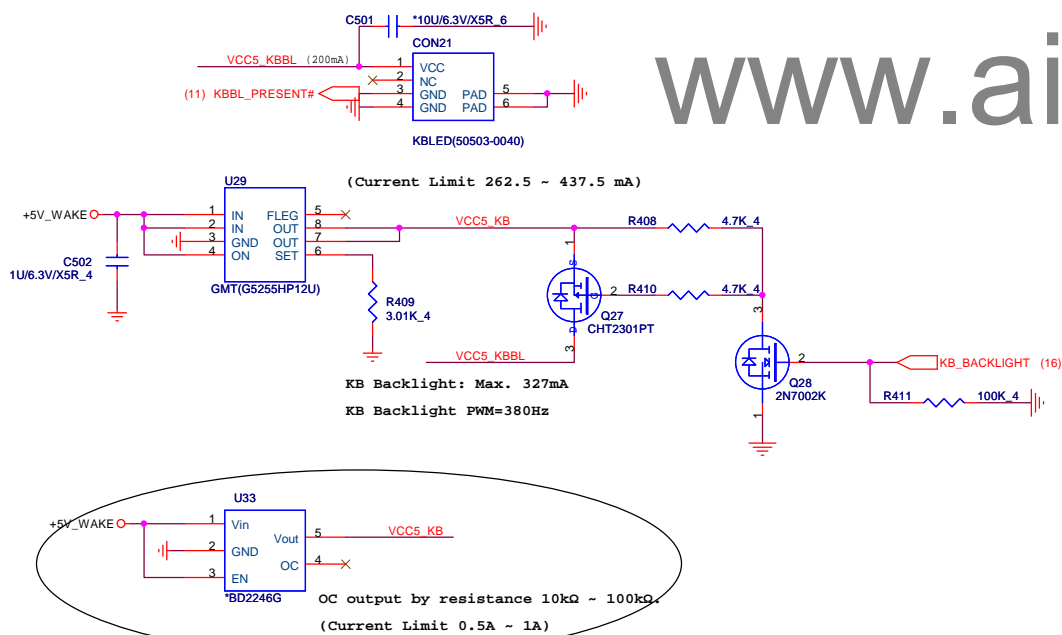
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WLAN/WIMAX/WIDI



KB BACKLIGHT



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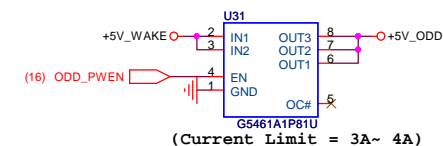
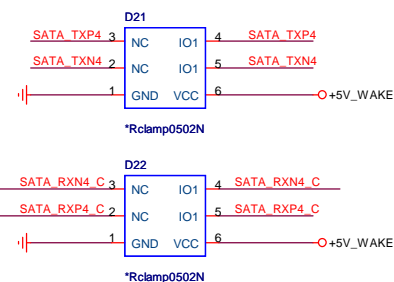
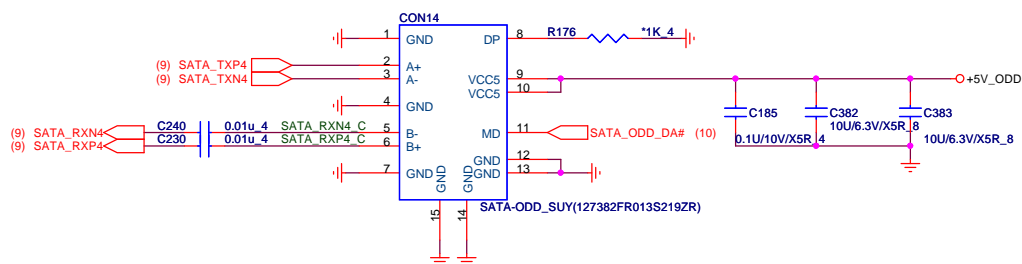
Quanta Computer Inc.

PROJECT : Chief River

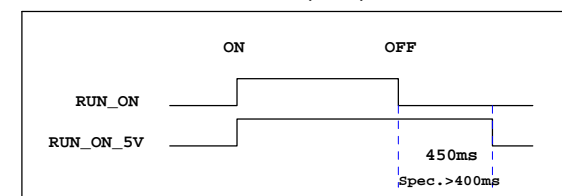
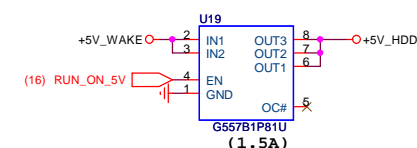
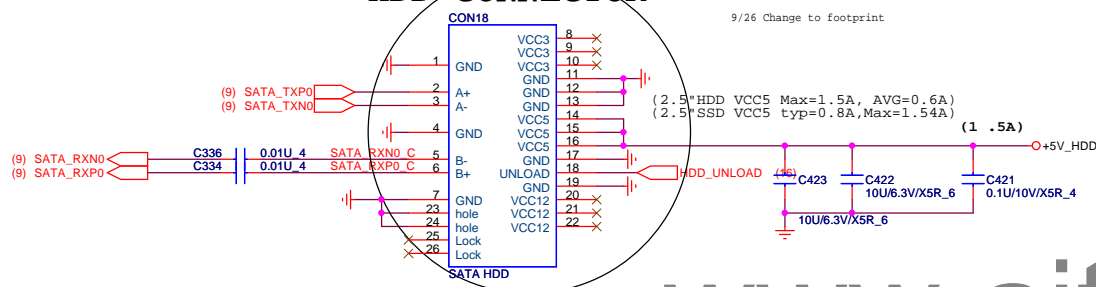
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	WLAN/KB BL	1A
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1. Level 1 Environment-related Substances Should Never be Used.
2. Recycled Resin and Coated Wire should be procured from Green Partners.

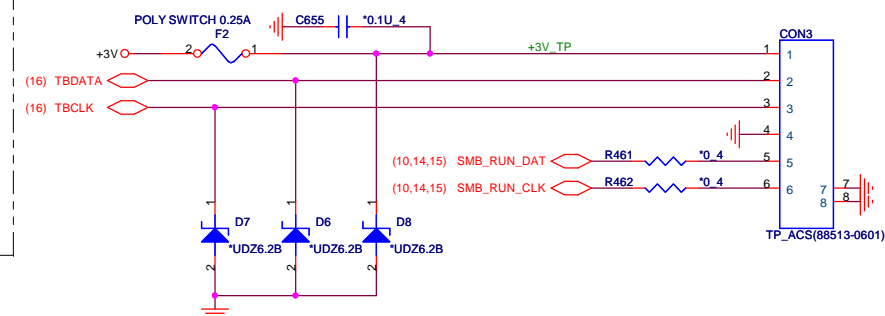
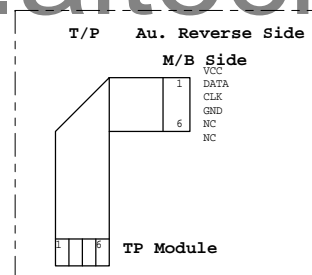
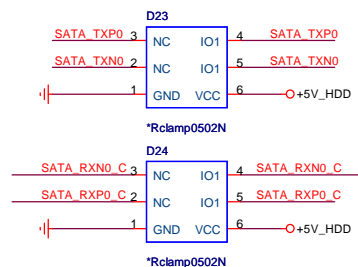
ODD CONNECTOR



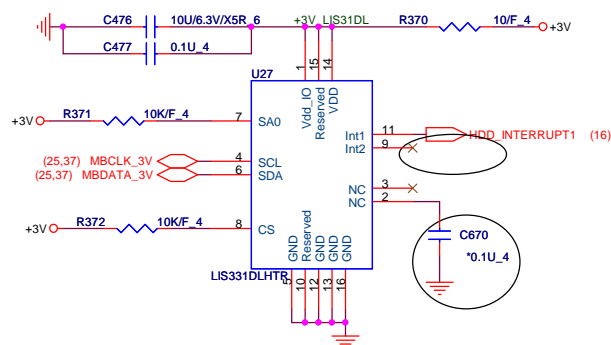
HDD CONNECTOR



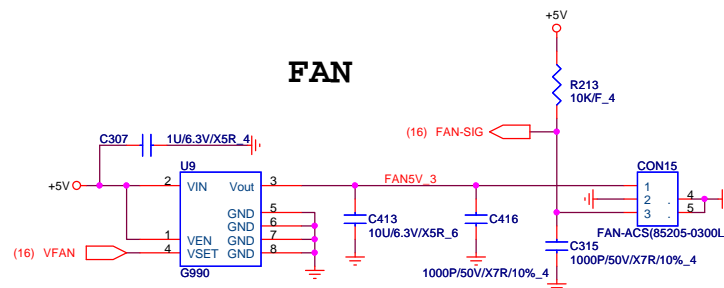
T/P Board to T/P

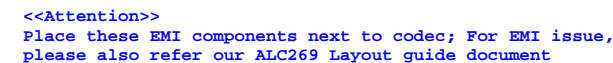


HDD PROTECT

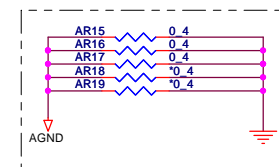


FAN



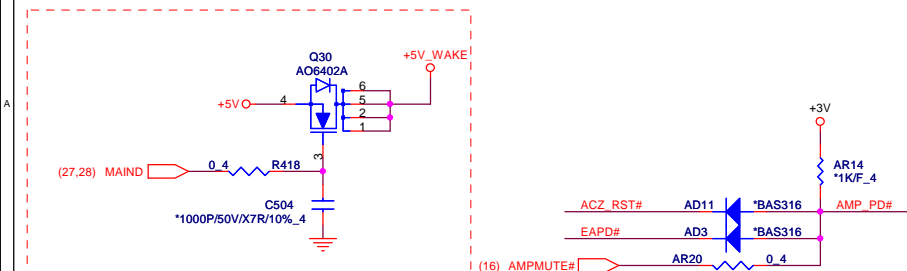
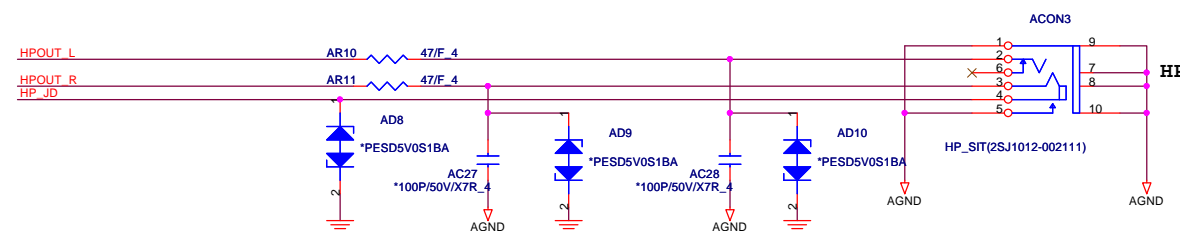
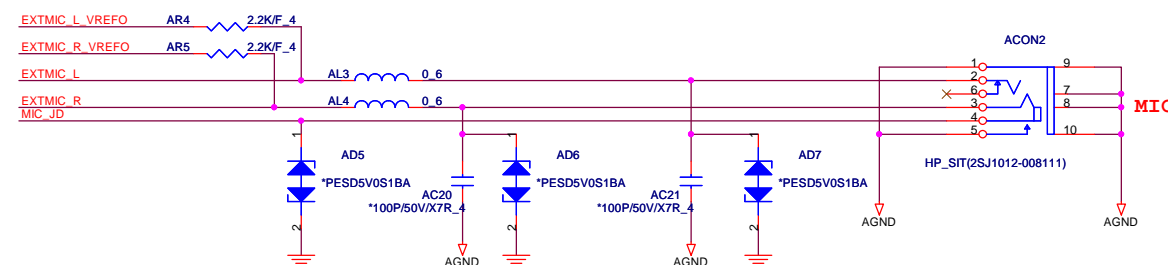


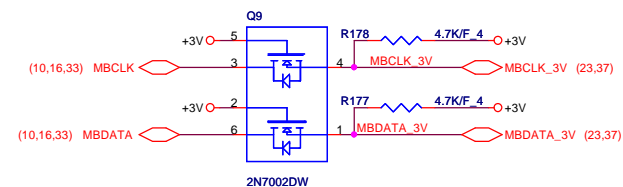
~~For EMI~~



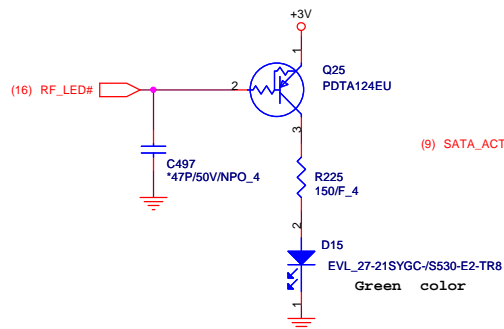
Place close Audio Codec


 Analog
 Digital

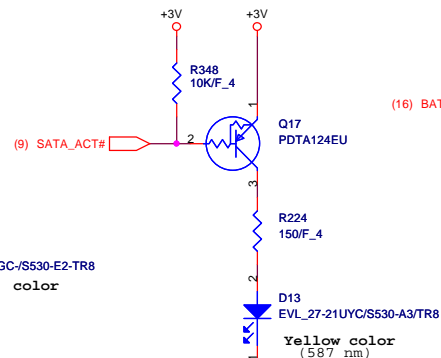




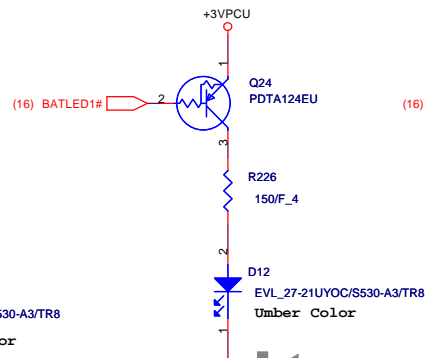
RF LED



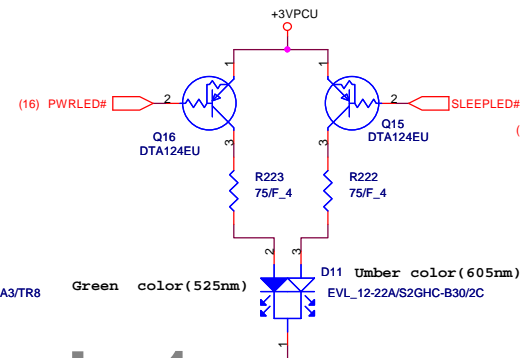
SATA LED



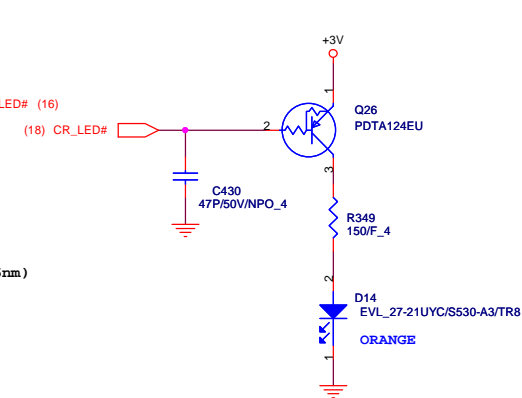
BATTERY LED



Power/Sleep LED

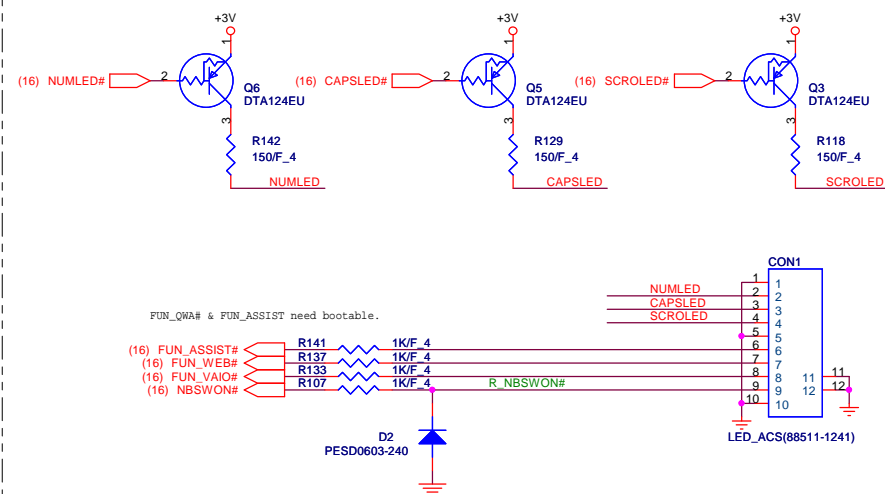


CARD LED



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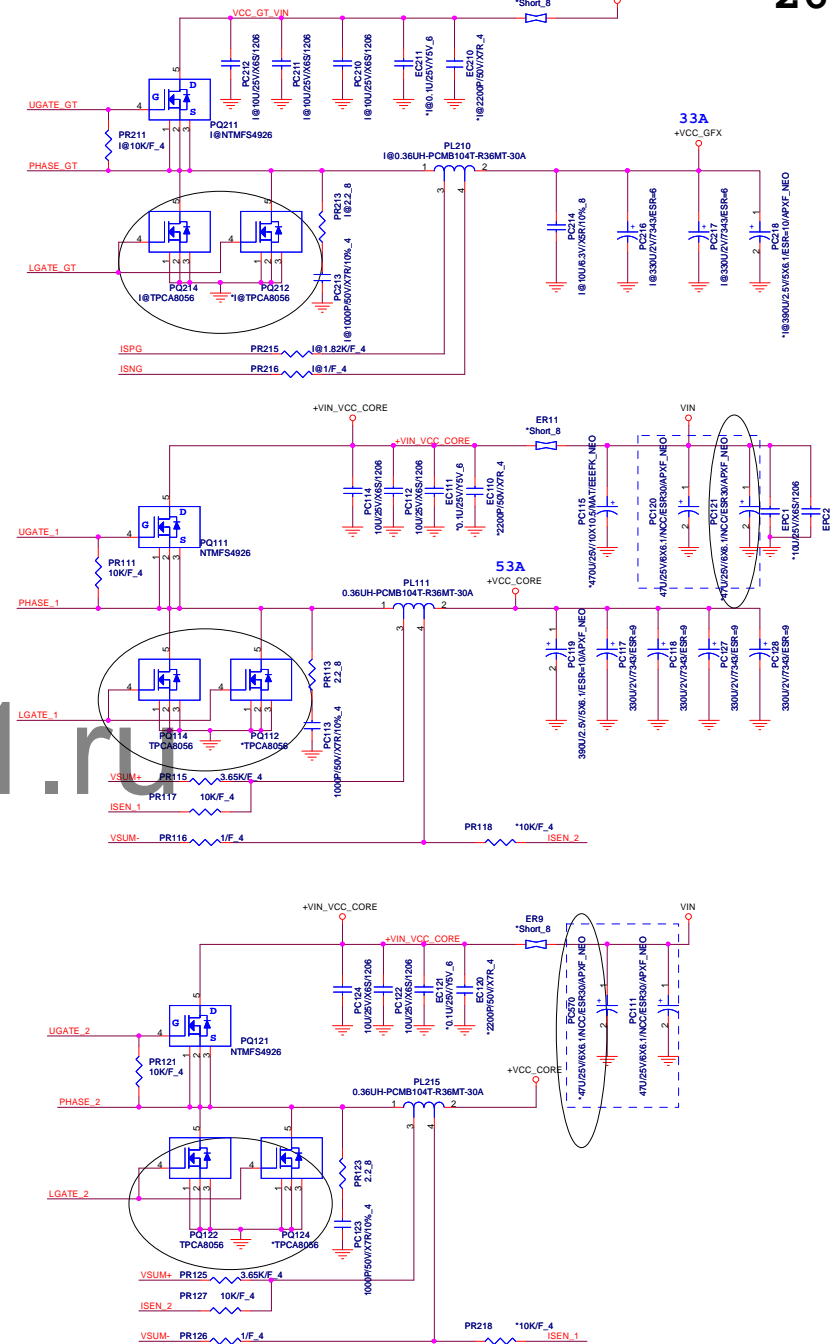
Power SW Board Connector



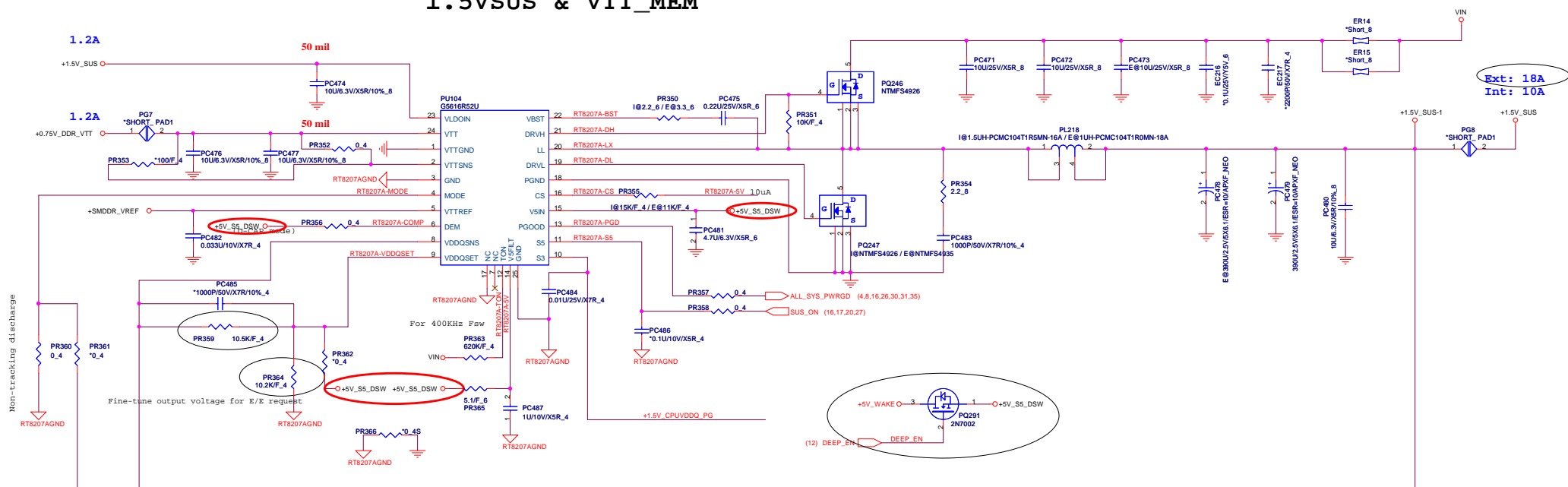
Quanta Computer Inc.
PROJECT : Chief River

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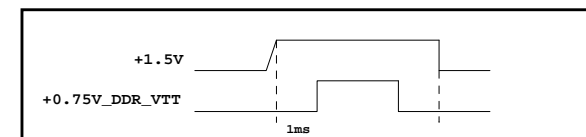
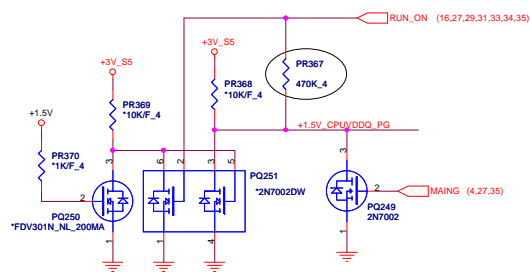
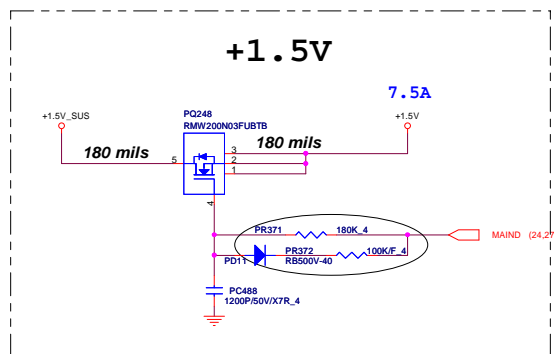
1. Level 1 Environment-related Substances Should Never be Used.
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1.5VSUS & VTT_MEM



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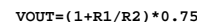


MODE	DISCHARGE MODE
+5V	No discharge
+1.5V	Tracking discharge
GND	Non-tracking discharge

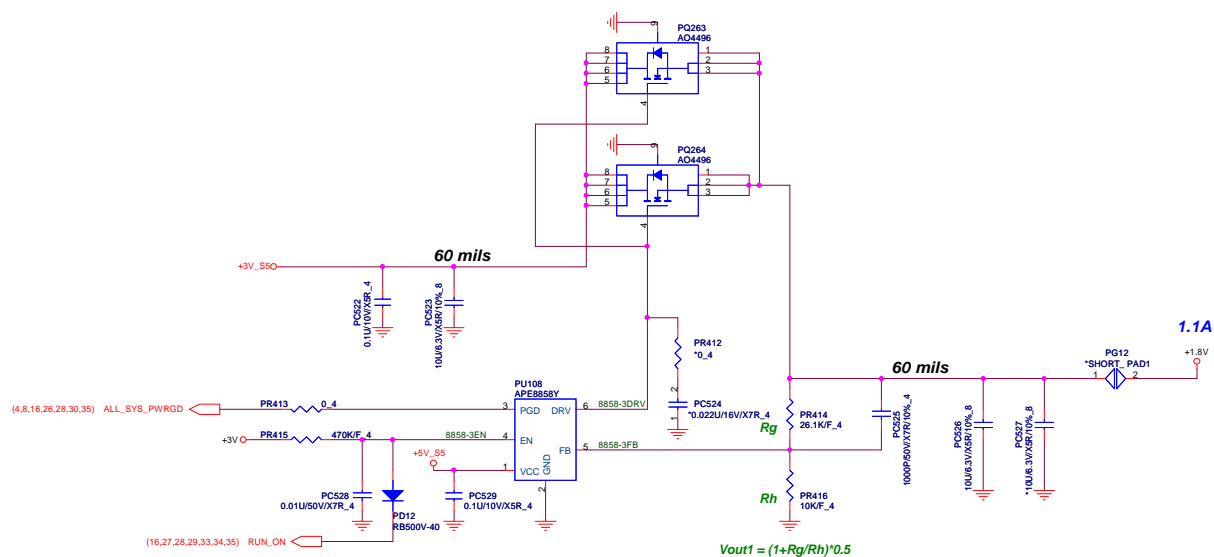
VDDQSET	VDDQ(V)	VTTREF & VTT	NOTE
GND	1.5 fixed	VDDQSNS/2	DDR3
5V	1.8 fixed	VDDQSNS/2	DDR2
FB-Resistor	Adjustable	VDDQSNS/2	1.5V<VDDQ<3V

$$V_{TT} = V_{TTREF} = V_{DDQSNS}/2 = 0.75V$$

STATE	S3	S5	1.5VSUS	VTTREF	VTT
S0	1	1	on	on	on
S3	0	1	on	on	off
S4/S5	0	0	off	off	off

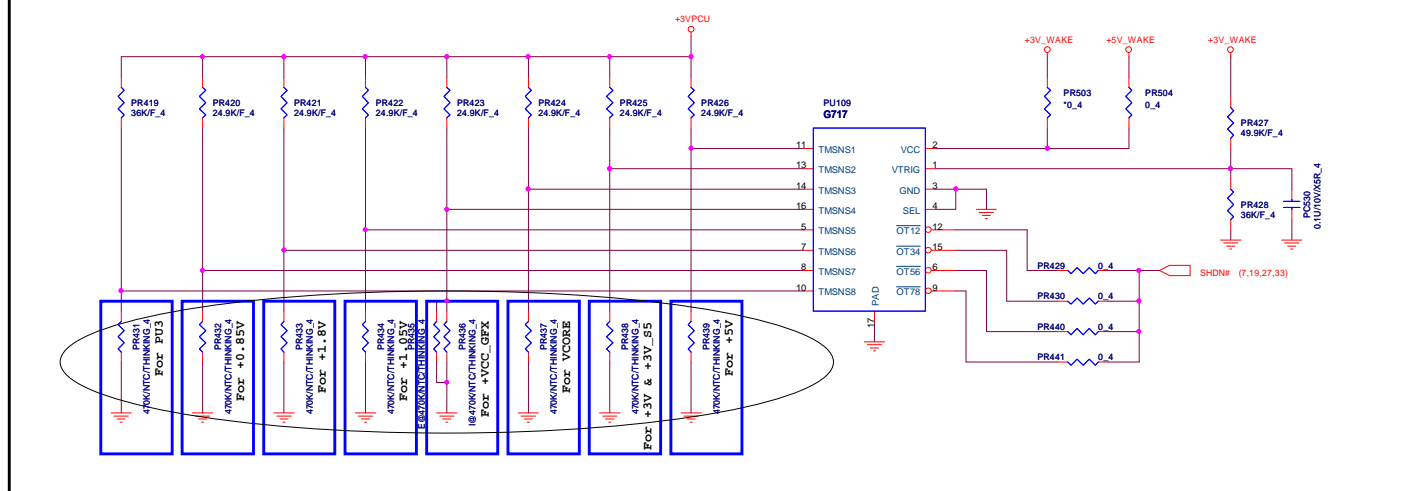


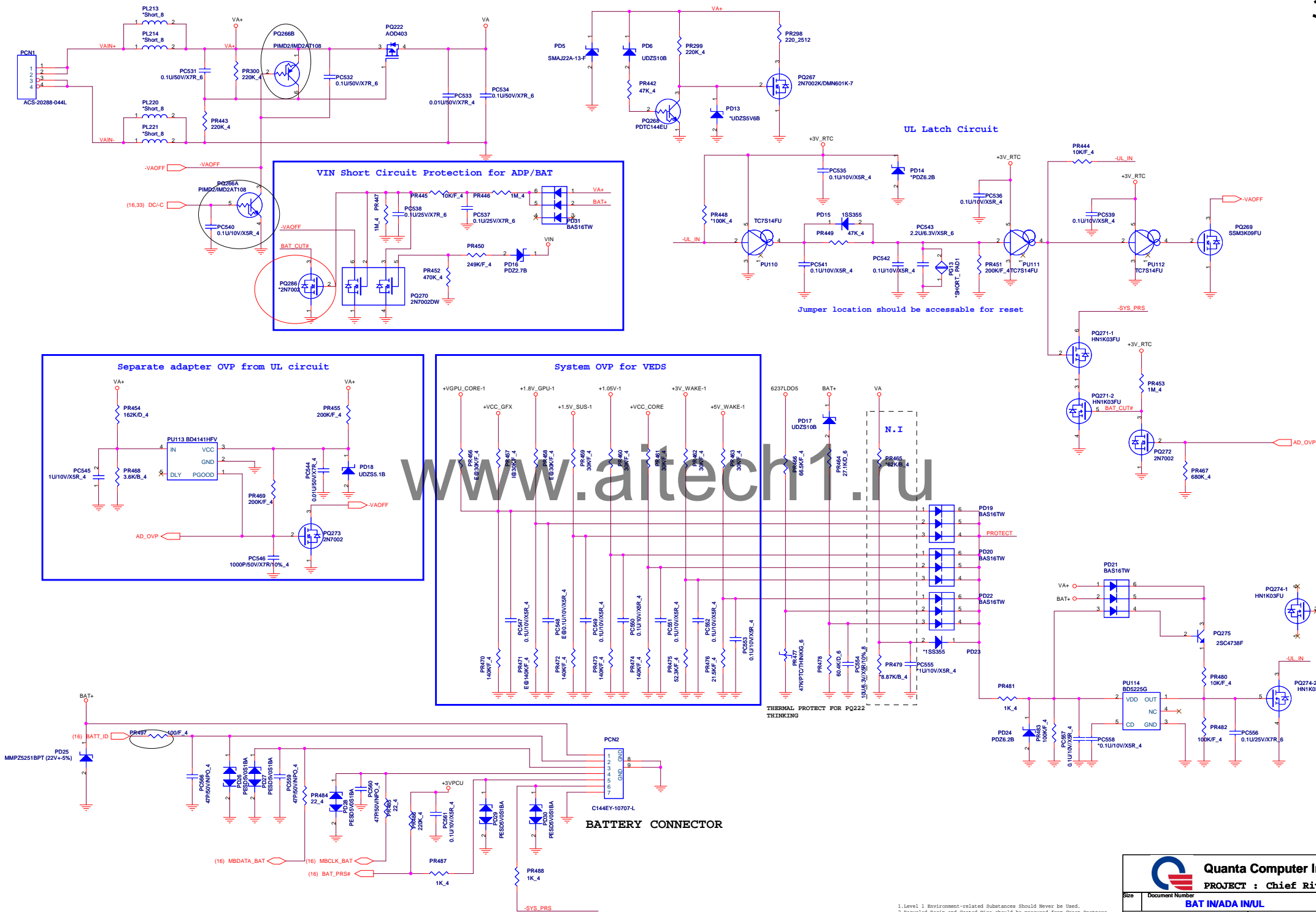
VCC1.8

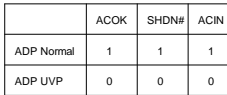


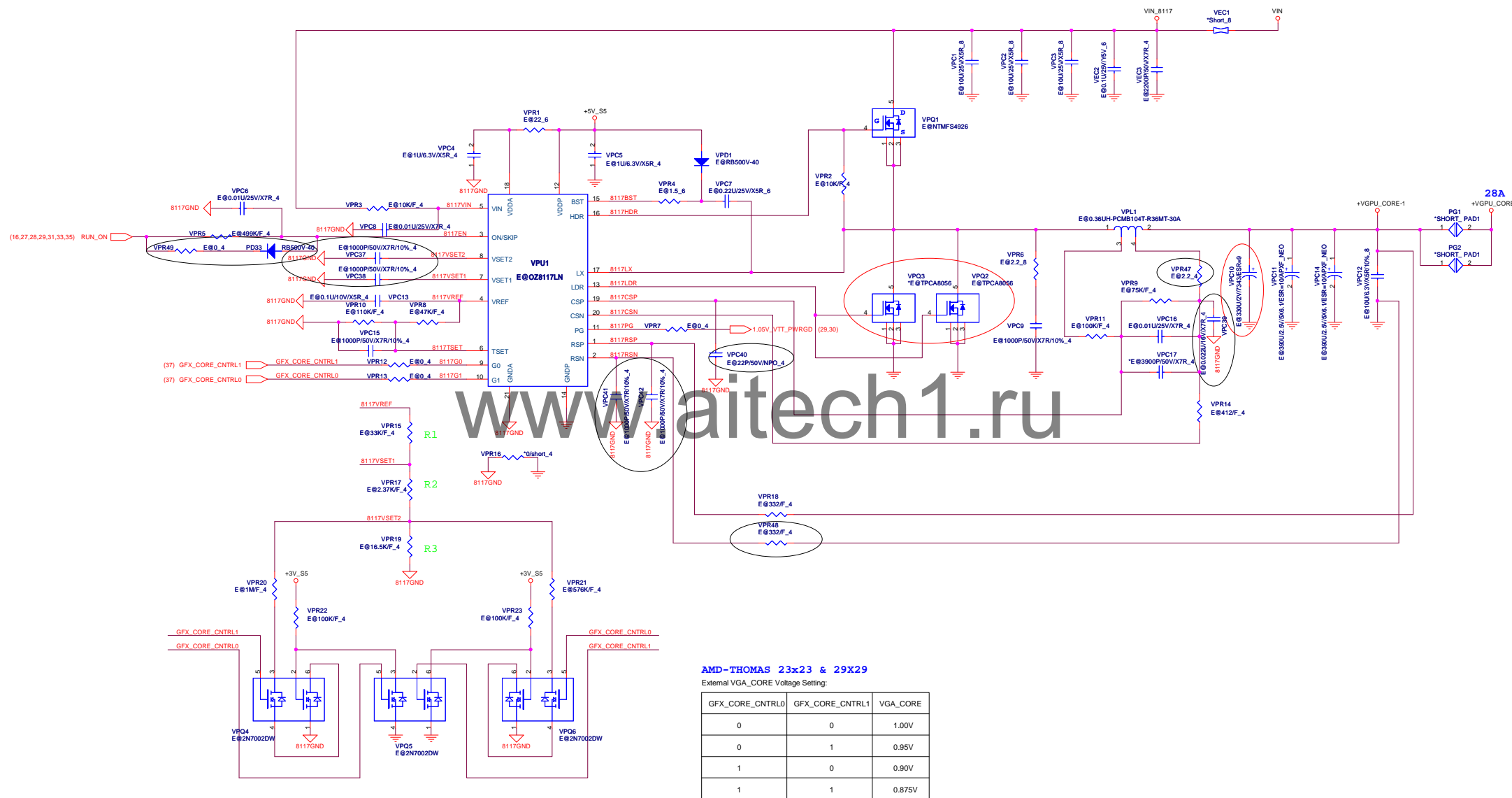
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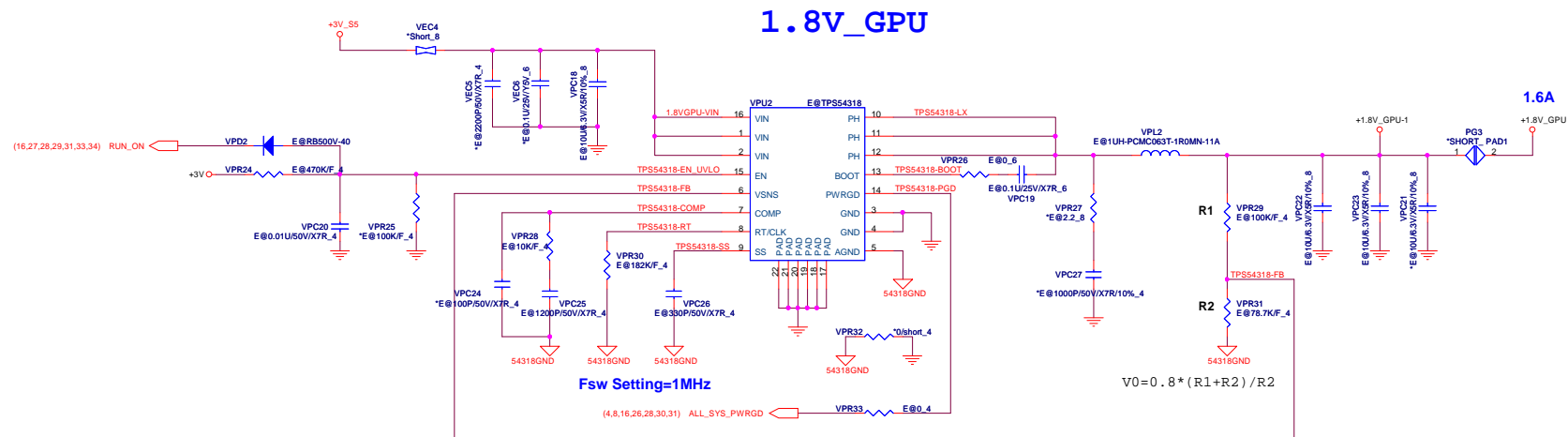
Thermal Protection for VEDS





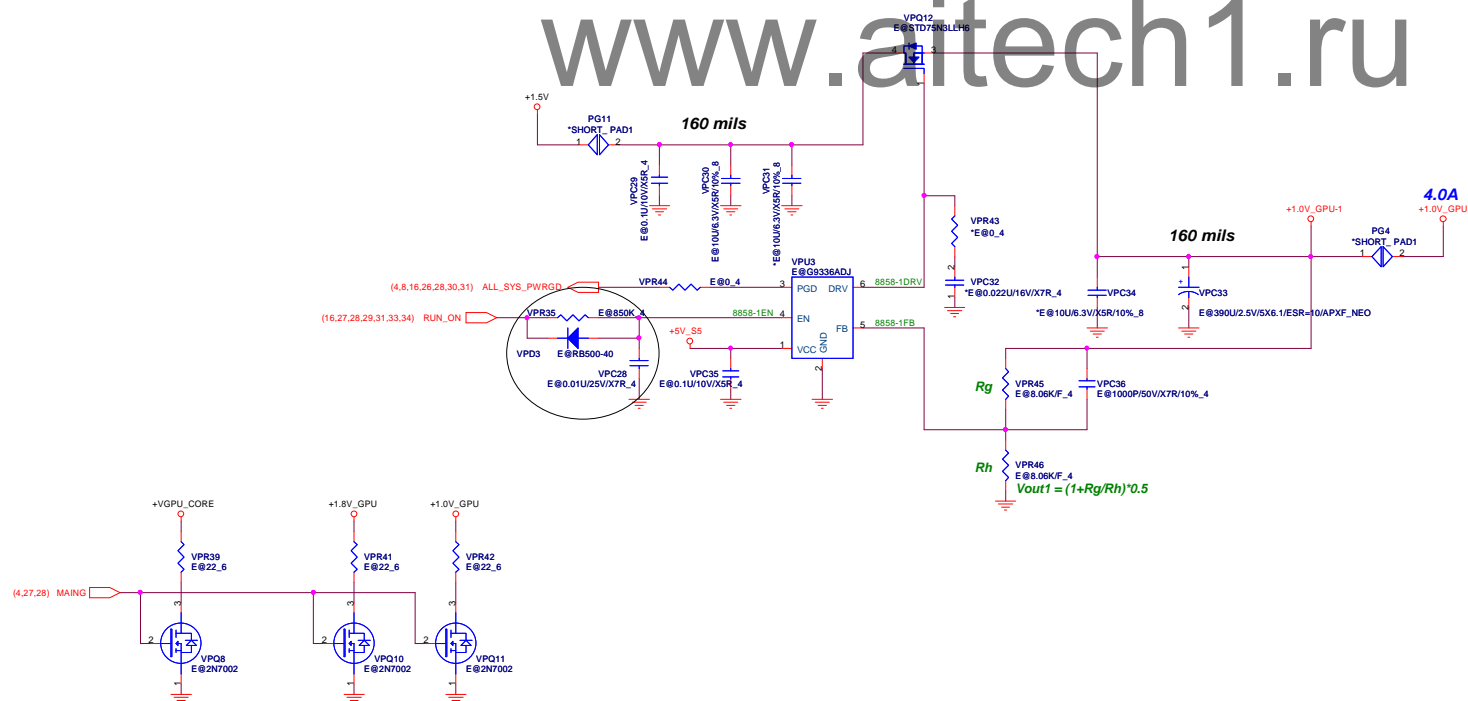


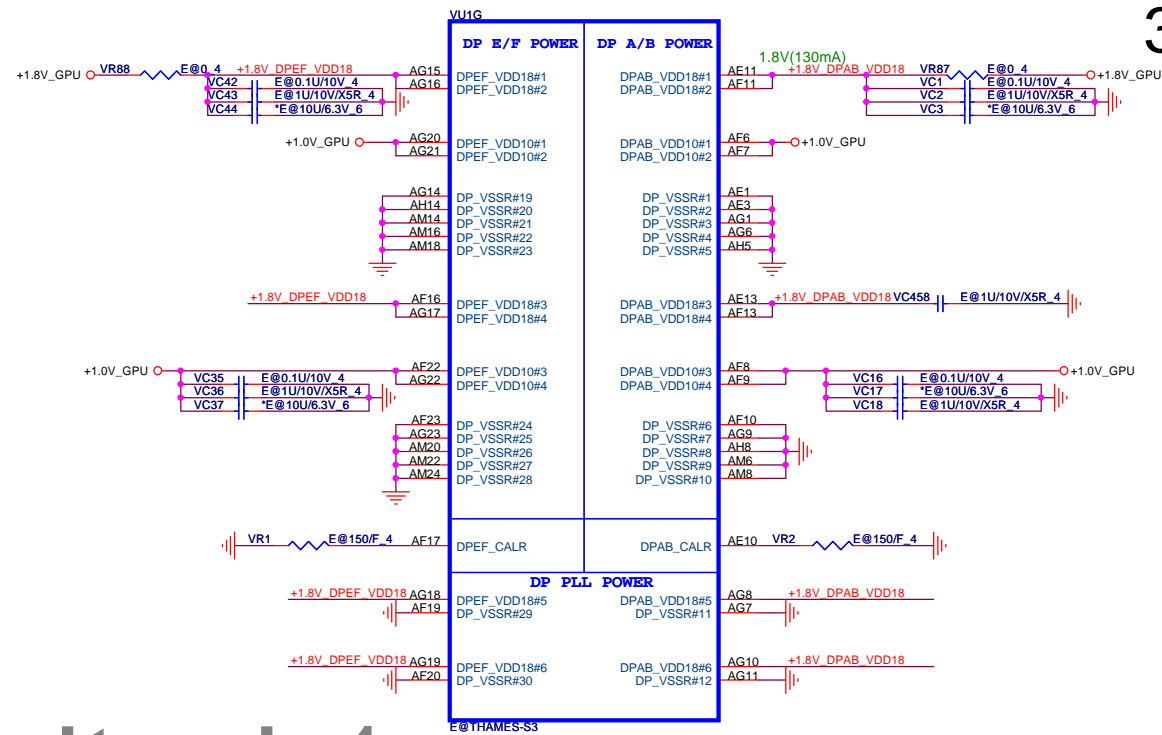
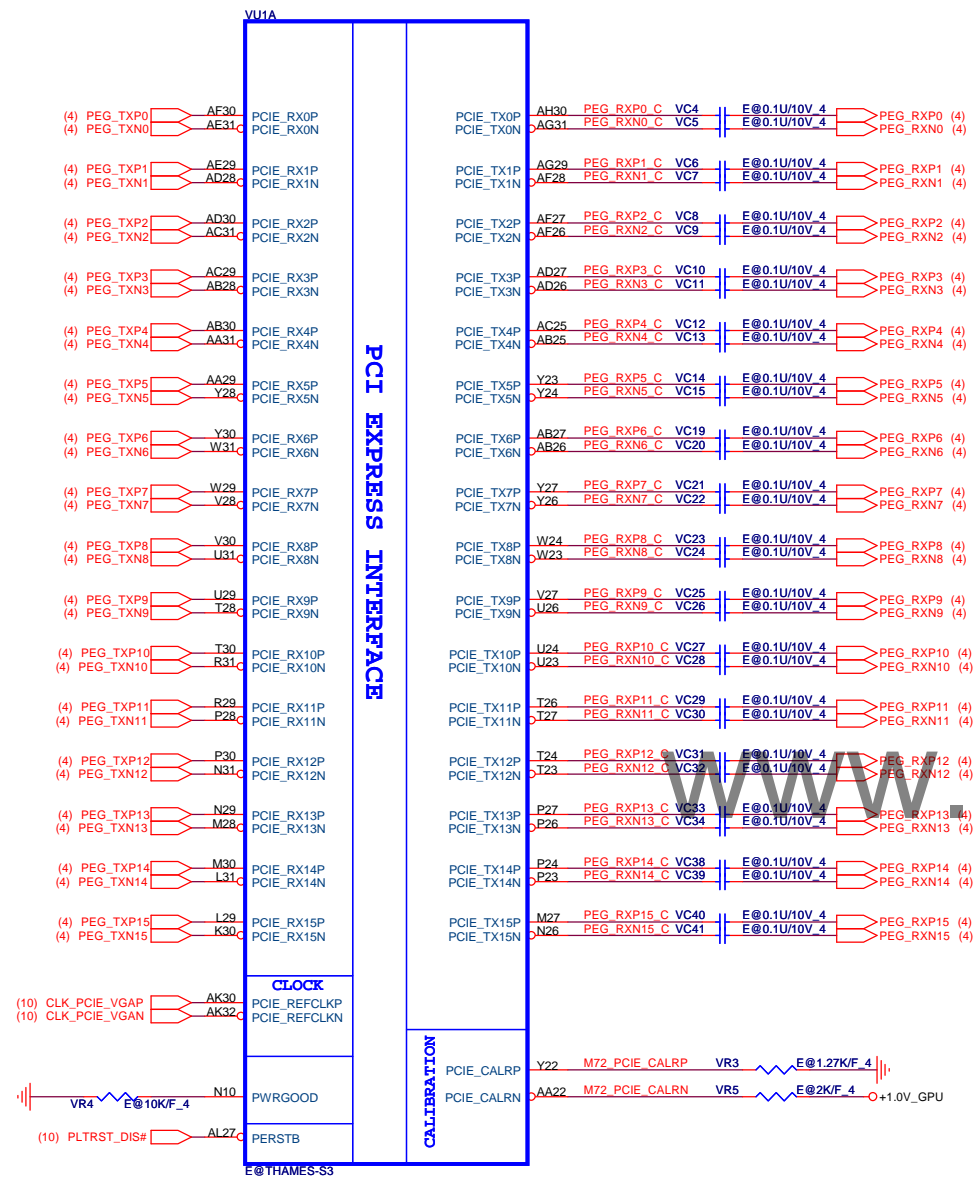




+1.0V_GPU (Support VRAM 900MHz)

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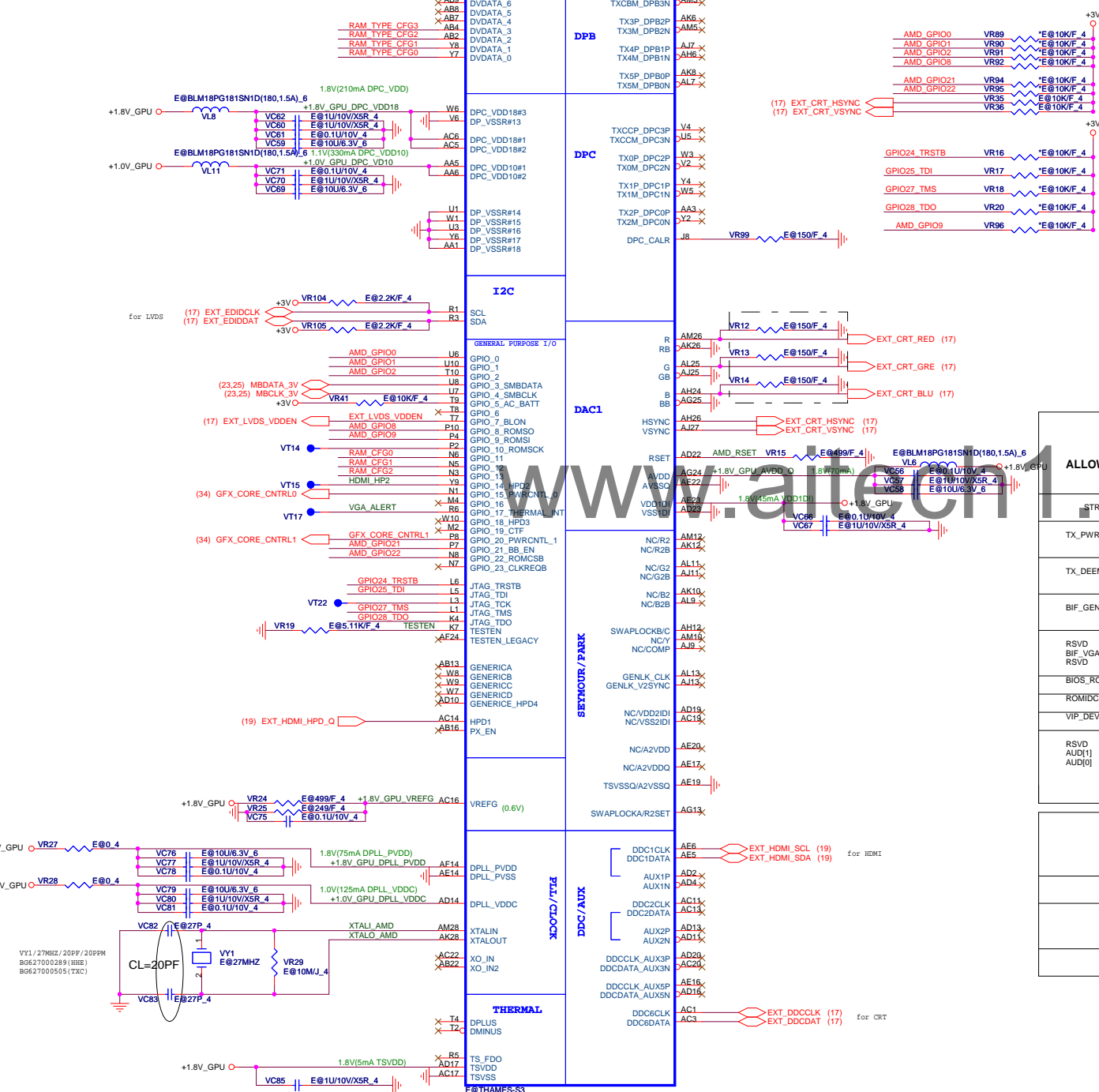


100MHz (+/-300ppm) Input Frequency
0-0.7V single-ended swing

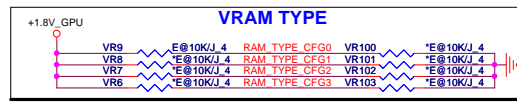


Quanta Computer Inc.
PROJECT : Chief River

	PWRCNTL0	PWRCNTL1	V-CORE
L	0	0	1.0V
M	0	1	0.95V
H	1	0	0.9V
TBD	1	1	0.875V



Memory Straps	MCLK:900Mhz	RAM TYPE_CFG3	RAM TYPE_CFG2	RAM TYPE_CFG1	RAM TYPE_CFG0
900 MHz 2Gb(128M*16) Hynix_Vega die	H5TQ2G63BFR-11C	0	0	0	0
900 MHz 2Gb(128M*16) Samsung_C die	K4W2G1646C-HC11	0	0	0	1
900 MHz 1Gb(64M*16) Hynix_Vega die	H5TQ1G63DFR-11C	0	0	1	0
900 MHz 1Gb(64M*16) Samsung_G die	K4W1G1646G-BC11	0	0	1	1



APERTURE SIZE

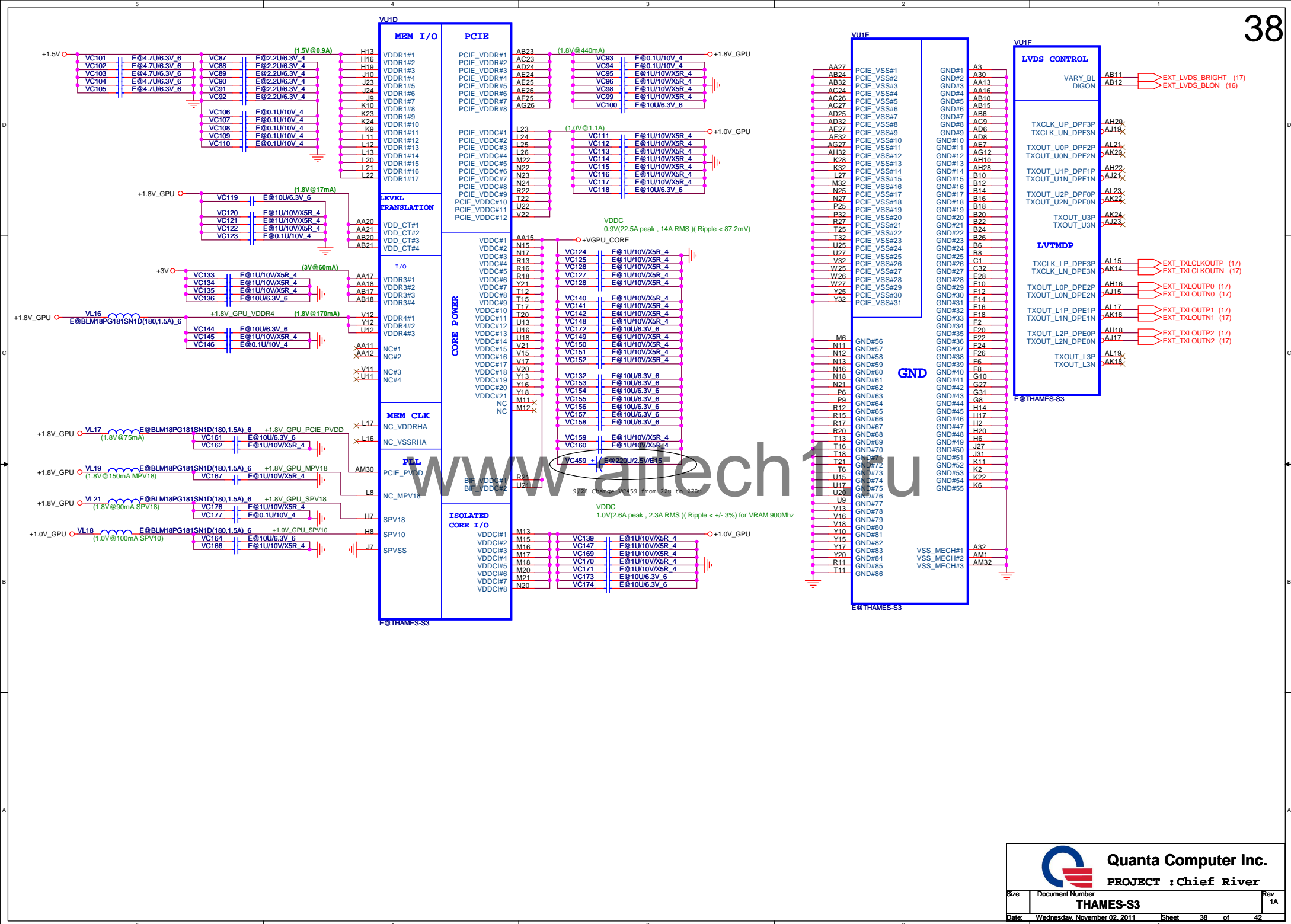
Database mean : 512MB 1GB memory setting should be 256MB

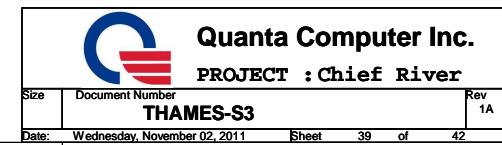
It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

MEMORY SIZE	CFG2 GPIO13	CFG1 GPIO12	CFG0 GPIO11
128MB	0	0	0
256MB	0	0	1
64MB	0	1	0

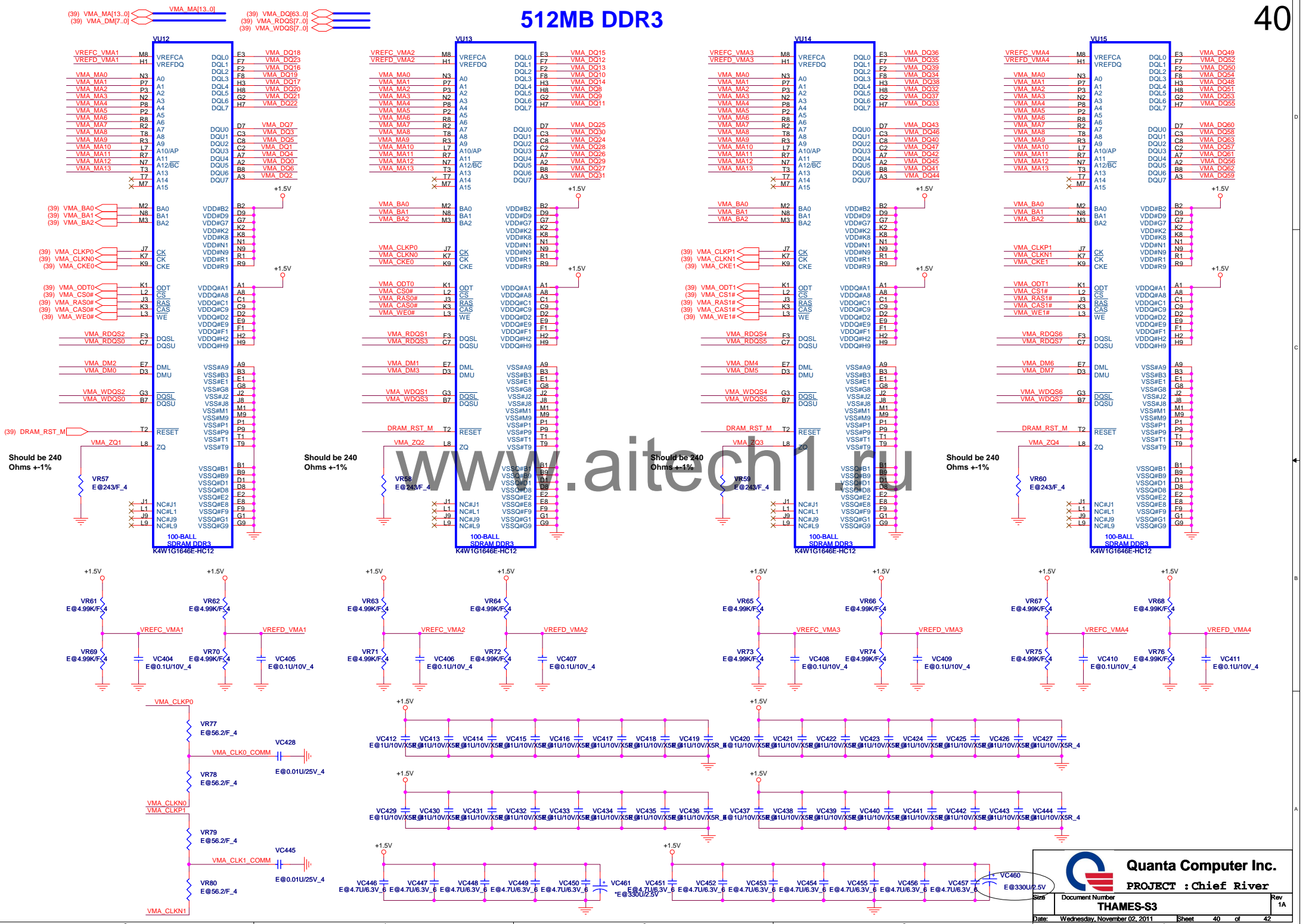
CONFIGURATION STRAPS			RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1= INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	0
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	0
BIF_GEN2_EN_A	GPIO2	Enable CLKREQ# Power Management 0: CLKREQ# power management capability is disabled 1: CLKREQ# power management capability is enabled	1
RSVD BIF_VGA_DIS	GPIO8 GPIO9 GPIO21	VGA ENABLED	0 0 0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD AUD[1] AUD[0]	GENERICC HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	0 0 11

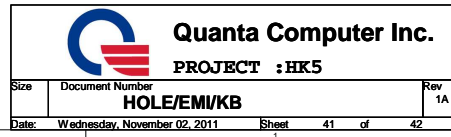
AMD RESERVED CONFIGURATION STRAPS		
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET		
H2SYNC	GENERICC	
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET		
GPIO21_BB_EN		





512MB DDR3





USB PORT Architecture for EVT	
PORT 0	IO Port
PORT 1	IO Port
PORT 2	IO Port
PORT 3	N/A
PORT 4	IO Port
PORT 5	N/A
PORT 6	N/A
PORT 7	N/A
PORT 8	N/A
PORT 9	WiMax/BT
PORT 10	Camera
PORT 11	N/A
PORT 12	N/A
PORT 13	N/A

PCIE BUS	
PORT 1	WLAN Port
PORT 2	CARD READER
PORT 3	GLAN(RTL8111E)
PORT 4	N/A
PORT 5	N/A
PORT 6	N/A
PORT 7	N/A
PORT 8	N/A

SATA BUS	
PORT 0	HDD
PORT 1	N/A
PORT 2	N/A
PORT 3	N/A
PORT 4	ODD
PORT 5	N/A

SM BUS	MBCLK/MBDATA	Function
ISL88731CHRTZ	0001 001X	Charger
AMD Thames	0100 0001	Graphice
LIS331DL	0011 001X	G Sensor

	R363(High) R362(Low)	R294(High) R297(low)
	Board ID3	Board ID0
14"/HK6	0	0
15"/HK5	0	1
17"/HK7	1	0

Board ID1 (VRAM Vendor)	Samaung(1)	Hynix(0)
R47(High)	Stuff	No Stuff
R48(Low)	No Stuff	Stuff

Board ID2		
14" 4PCS	1G	512M
15" 8PCS	1G	2G
R39(High)	Stuff	No Stuff
R27(Low)	No Stuff	Stuff

PCBA SKU	Discrete	UMA
R277(Pull High)	Stuff	No Stuff
R275(Pull Low)	No Stuff	Stuff

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